PAC22140 Data Sheet

10S-20S Smart BMS with Integrated MCU and Cell Balancing

Product Overview

The Qorvo® PAC22140 is a Smart Battery Monitoring System (BMS) that can monitor 10-series to 20-series Li-Ion, Li-Polymer and LiFePO4 battery packs.

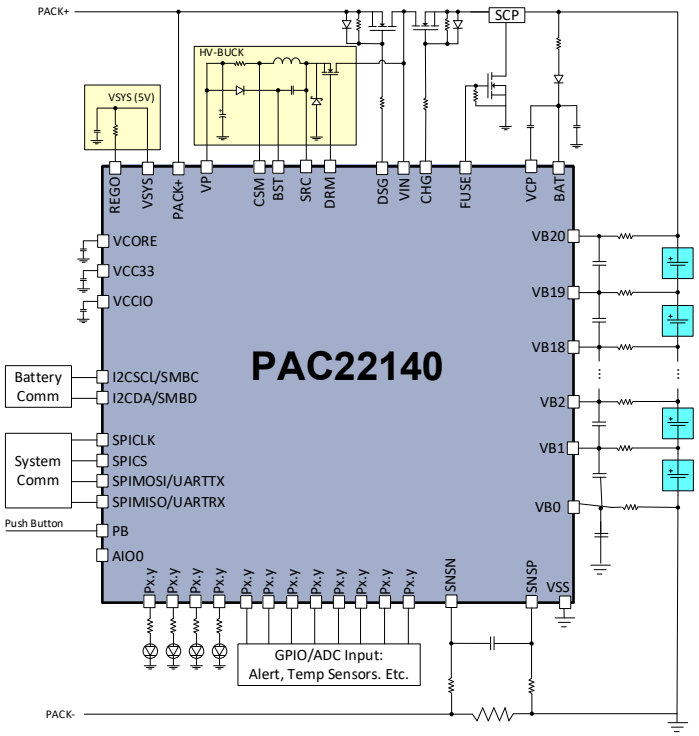
The PAC22140 integrates a FLASH-programmable MCU, Power Management, Current/Voltage/Temperature Sense and drive circuits for charge/discharge FETs and protection fuses. It can communicate using UART/SPI or I2C/SMBus serial interfaces.

The PAC22140 contains an Arm® Cortex®-M0 with 32kB of FLASH and 8KB of SRAM and has access to several different analog and digital peripherals that is intended to be used for the fuel gauging algorithm and system telemetry reporting.

There is a single supply 145V input Buck DC/DC controller, used to generate gate drive voltages for external charge and discharge FETs and external FUSE FET, as well as all the sub-regulators required for the MCU and other sub-systems in the device. There are high-side gate drivers for a charge and discharge FET, as well as a low-side driver to blow a battery pack fuse.

The device also integrates a programmable-gain differential amplifier and 16-bit Sigma-Delta ADC for current sense as well as a 16-bit Sigma-Delta ADC for cell balancing voltage sense and a 10-bit SAR ADC for additional voltage and temperature sense usage.

The PAC22140 is packaged in an 9x9mm, 60-pin QFN package for compact, high cell count battery-monitoring applications.



Key Features

MCU

- 50MHz Arm® Cortex®-M0
  - 32kB FLASH
  - 8kB SRAM
  - 256B INFO FLASH for manufacturing information
  - 20 interrupts, 4 priority levels
- SWD programming interface
- Clock-gating for low-power operation

MCU ADC

- 10-bit 1MSPS SAR ADC
- Dual 8-channel ADC sequencer

Timing Generators

- Four 16-bit PWM timers with up to 8 CCR output units each
- 24-bit SysTick count-down timer
- Watch-dog Timer (WDT)
- AFE Windowed Watch-dog Timer (WWDT) running off independent clock

IO

- 3.3V/5V configurable drive output
- 17 general-purpose IO
- Digital Input, digital output, analog ADC input
- Configurable weak pull-up or pull-down
- Configurable drive-strength (8mA or 16mA)
- Flexible interrupt controller

Communication Peripherals

- UART or SPI and I2C/SMBus
- 8-bit UART, up to 1Mbps
- 3-wire or 4-wire SPI, master/slave
- I2C master/slave, 7b/10b
- Single-wire debugger (SWD)

Power Manager

- Up to 145V supply input Buck DC/DC Controller
  - OC, OV and UV protection
- High-Voltage Charge Pump
- 5V/225mA system regulator
- Integrated LDOs for analog, IO, and core supplies
- Power and temperature monitor, warning, and fault detection
- Low-Power Operation
  - 3µA total hibernate mode
  - Push Button, PACK+ Charger Detect, and Timer wakeup modes

Configurable Analog Front-End (CAFE™)

- Programmable-Gain Differential amplifier and 16-bit Sigma-Delta ADC for battery pack current sense
- 16-bit Sigma-Delta ADC for voltage sense
- Integrated ADC references
- Programmable over-current shutdown
- Power supply monitoring via ADC
- Low-speed independent clock source

Application Specific Power Drivers (ASPD™)

- Integrated high-side gate drivers for external CHG and DSG FETs
- Integrated low-side gate driver for pack FUSE blow FET

Integrated Cell Balancing

- Cell balancing for up to 20 cells

Packaging

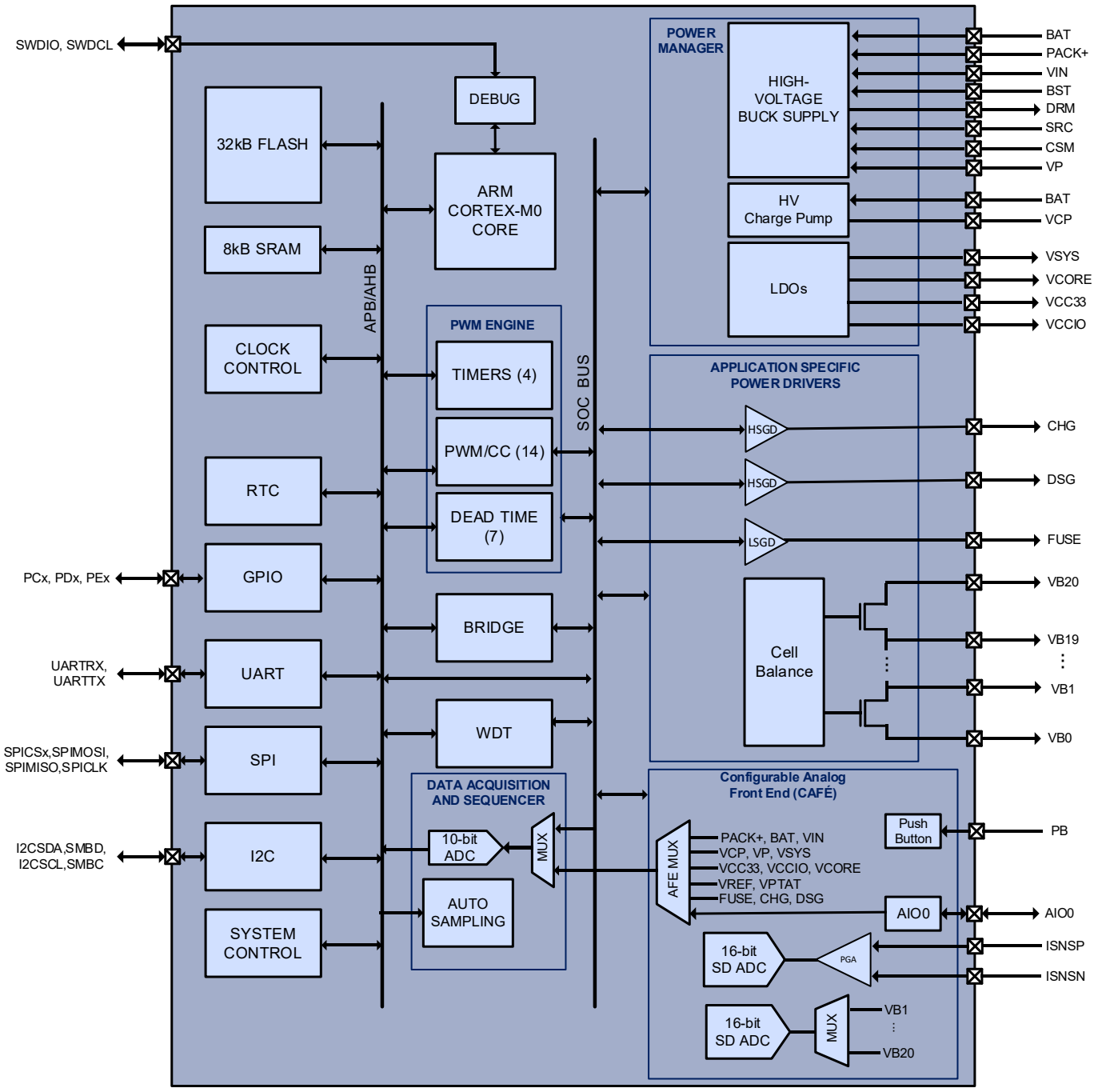
- QFN 9x9mm 60-pin package, 0.5mm pitch
- Exposed pad for thermal management

Certifications

- T_A = -40°C to 105°C

Functional Block Diagram

Figure 1 Architectural Block Diagram



Ordering Information

ORDERABLE PART NUMBER	UNIT QUANITY	MCU	FLASH	SRAM	CELL COUNT	GPIO	PACKAGE
PAC22140SR	100 unit short reel	50MHz ARM Cortex M0	32kB	8kB	10 to 20	17	QFN 9x9mm 60-pin
PAC22140-T	3000 unit reel						

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Absolute Maximum Ratings

Symbol	Value	Unit
Power Manager		
VCP to BAT	-0.3 to 14	V
VIN, BAT, PACK+ to VSS	-0.3 to 145	V
BST to VSS	-0.3 to 145	V
BST to SRC	-0.3 to 20	V
SRC to VSS	-5 to VIN + 15	V
DRM to SRC	-0.3 to 20	V
VP to VSS	-0.3 to 14	V
CSM to VP	-0.3 to 0.3	V
VSYS to VSS	-0.3 to 6	V
REGO to VSS	-0.3 to VP + 0.3	V
VCC33 to VSS	-0.3 to 4.1	V
VCCIO to VSS	-0.3 to VSYS	V
VCORE to VSS	-0.3 to 2.5	V
Signal Manager		
ISNSP, ISNSN to VSS	-0.3 to +0.3	V
Cell Balancing		
VB[n] to VSS	(n+1) * 6.9	V
VB[n+1] to VB[n]	-0.3 to 10	V
Driver Manager		
CHG, DSG to VSS	-0.3 to 145	V
CHG to BAT	-0.3 to 14	V
DSG to PACK+	-0.3 to 14	
FUSE to VSS	-0.3 to 14	V
IO		
PDx, PEx to VSS	-0.3 to VCCIO + 0.3	V
PCx to VSS	-0.3 to VCC33 + 0.3	V
I_{Pxy} pin injection current	7.5	mA
$\sum I_{Pxy}$ sum of all pin injection current	25	mA
Temperature		
T_A	-40 to 105	°C
T_{STG}	-55 to 150	°C
Electro-static Discharge (ESD)		
Human Body Model (HBM)	1	kV
Charge Device Model (CDM)	500	V

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
PACK+	Charger Input Voltage	18		100	V
BAT	Battery Stack Voltage	18		100	V

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

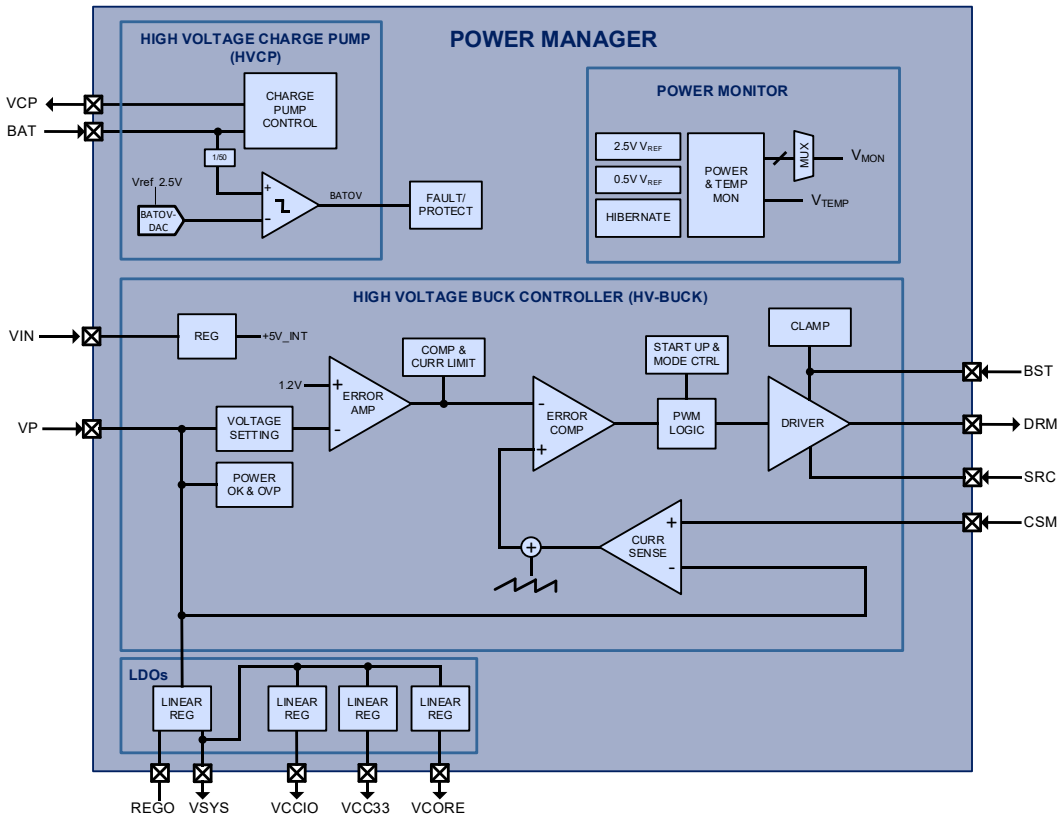
Power Manager

Features

- 145V Single Supply High-Voltage Buck (HV-BUCK) DC/DC controller
- High-Voltage Charge Pump
- 5V/225mA VSYS regulator for system supply
- VCC33 LDO for 3.3V analog supply
- VCCIO LDO for 3.3V IO supply
- VCORE LDO for 1.8V core supply
- High-accuracy 2.5V voltage reference for MCU ADC (VREF)
- High-accuracy 0.5V voltage reference for Current Sense ADC
- Power and temperature monitoring, warning, and fault detection
- Extremely low hibernate mode I_Q of 3µA Typical at VIN=80V

Block Diagram

Figure 2 Power Manager Block Diagram



Functional Description

The Power Manager is optimized to efficiently provide “all-in-one” power management required by the PAC22140 and associated application circuitry. It incorporates a 145V input High-Voltage Buck DC/DC (HV-BUCK) and High-Voltage Charge Pump (HVCP) to generate the supplies for the integrated gate drivers and other sub-regulators.

The VSYS LDO generates a 5V/225mA system supply that is used to power the IC and the other LDOs. VSYS is used to supply the VCC33, VCCIO and VCORE, which are used to generate a 3.3V analog, 3.3V IO and 1.8V digital core supply.

The power manager also handles system functions including internal reference generation, timers, hibernate mode management, and power and temperature monitoring.

High-Voltage Buck (HV-BUCK)

The PAC22140 contains a High-Voltage Buck Controller for a Buck DC/DC (HV-BUCK). The HV-BUCK controller drives an external power MOSFET for pulse-width modulation switching of an inductor for power conversion. VIN is the HV-BUCK supply controller input. The DRM output drives the gate of the N-CH MOSFET between the VIN on state and VSS off state at proper duty cycle and switching frequency to ensure that the main supply voltage VP is regulated. The gate of the high-side power MOSFET is connected to the DRM pin and the source of the high-side power MOSFET is connected to SRC.

The VP regulation voltage is set to a fixed 12V. When VP is lower than the target regulation voltage, the internal feedback control circuitry causes the inductor current to increase to raise VP. Conversely, when VP is higher than the regulation voltage, the feedback loop control causes the inductor current to decrease to lower VP. The feedback loop is internally stabilized. The output current capability of the switching supply is determined by the external current sense resistor. The inductor current signal is sensed differentially between the CSM pin and VP and has a peak current limit threshold of 0.2V.

High-Voltage Charge Pump (HVCP)

The High-Voltage Charge Pump (HVCP) is used as the high-side gate drive supply for the external CHG and DSG FET gate drivers. The charge pump output is VCP and charges to BAT + 9V when enabled.

The BAT Over Voltage DAC (BATOVDAC) and comparator can be used to monitor the BAT voltage, and trigger faults and protection mechanisms.

HV-BUCK Restart Handling

The HV-BUCK has a safety re-start mechanism that protects the device and external components in case of a DC/DC failure. This mechanism samples VIN and VP when the HV-BUCK is re-started and may insert a delay before it allows the power supply to be re-started in case of some type of short or damage with the power supply components on the PCB.

If the DC/DC has been disabled due to VIN falling below $V_{UVLOF;VIN}$, VIN is sampled and as soon as VIN > $V_{UVLOR;VIN}$, then the DC/DC will immediately re-start.

If VIN is > VIN UVLO falling ($V_{UVLOF;VIN}$) but VP < VP UVLO falling ($V_{UVLOF;VP}$) then the DC/DC is disabled and a 350ms delay is inserted. After this delay, the DC/DC is re-started.

Linear Regulators

The PAC22140 includes four linear regulators:

- VSYS
- VCC33
- VCCIO
- VCORE

The system supply regulator (VSYS) is a medium-voltage regulator that is supplied by VP (output of HV-BUCK) and sources up to 225mA at REGO until VSYS, externally coupled to REGO, reaches 5V. This allows a properly rated external resistor to be connected from REGO to VSYS to close the current loop and offload power dissipation between VP and VSYS. The VSYS regulator supplies the VCC33, VCCIO and VCORE sub-regulators.

The VCC33 regulator generates a 3.3V analog supply for the ADC and GPIO on the MCU. The VCORE regulator generates a dedicated 1.9V digital logic supply for the MCU. The VCCIO regulator generates a dedicated 3.3V supply for the GPIO on the MCU. The GPIO on the MCU may also be driven at 5V by shorting VCCIO to VSYS on the PCB.

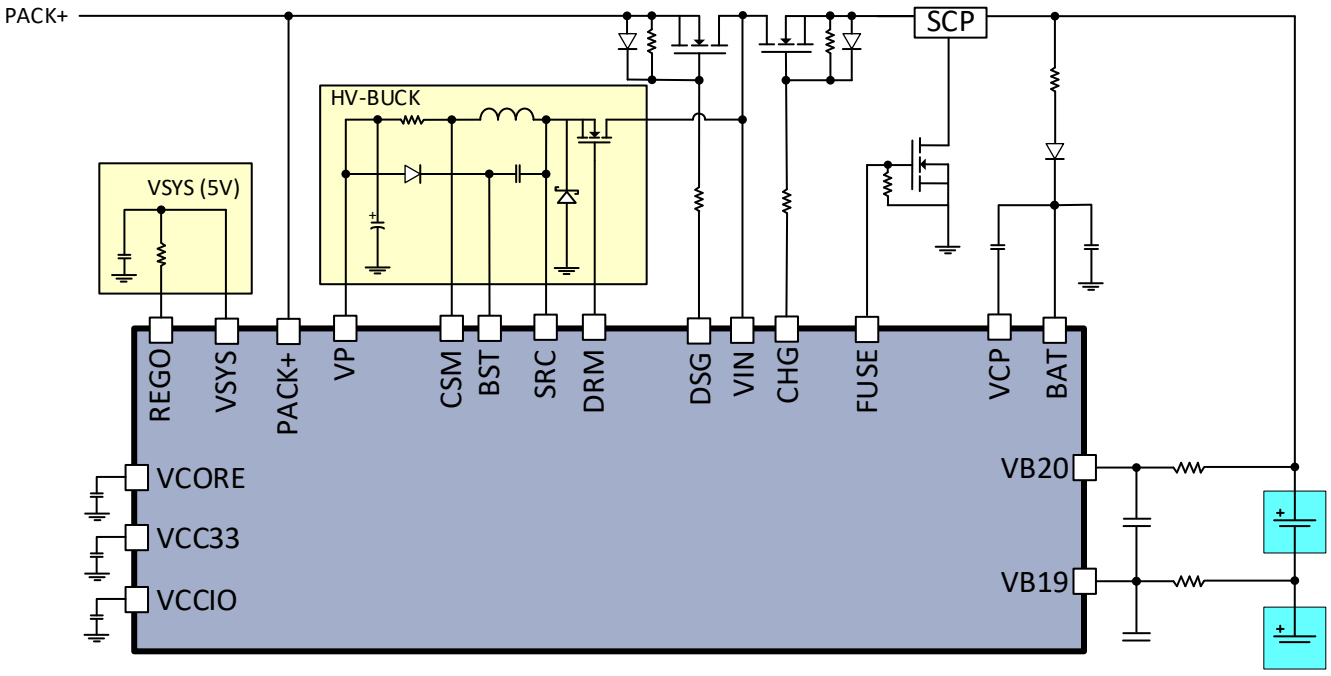
Once all LDOs are above their respective power good thresholds, then the MCU is released from reset and begins executing instructions.

Each of the LDOs must be bypassed externally to ground. See the electrical characteristics below for details on the recommended component values for each of the bypass capacitors.

Power Manager Circuit Connections

Figure 3 below shows the typical circuit connections for the HV-BUCK on the PAC22140.

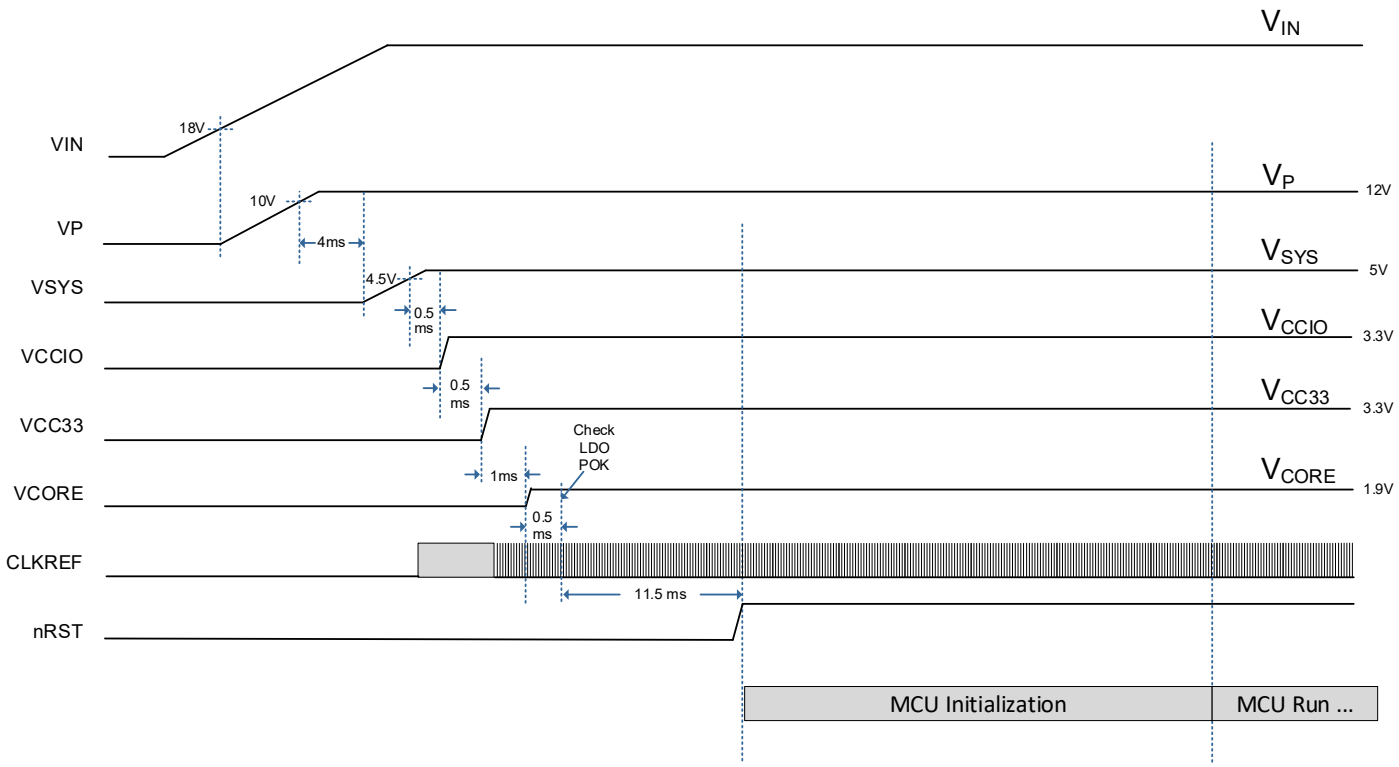
Figure 3 HV-BUCK Circuit Connections



HV-BUCK and LDO Power-up Sequence

The HV-BUCK and LDOs follow a typical power-up sequence as shown in Figure 4 below.

Figure 4 HV-BUCK and LDO Power-up Sequence



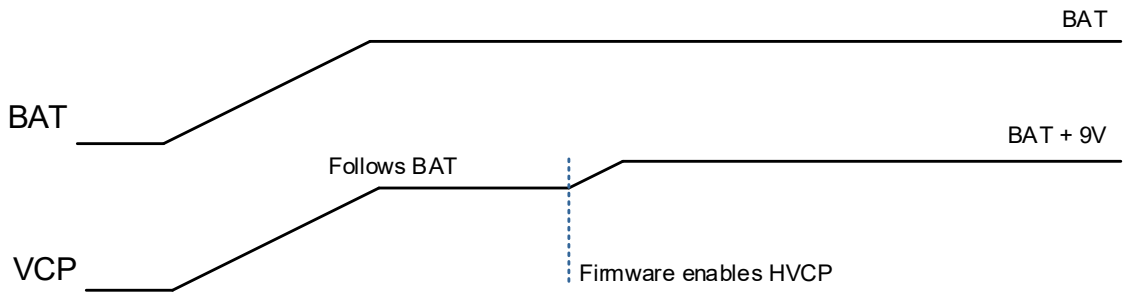
A typical sequence begins with voltage being applied on VIN. Once VIN reaches 18V, the HV-BUCK is enabled, and VP begins to rise. When VP reaches 10V, then after 4ms the VSYS regulator is enabled. When VSYS reaches its power good threshold of 4.5V, then after 0.5ms VCCIO is enabled. After another 0.5ms, VCC33 is enabled. Finally after another 1ms, VCORE is enabled.

The power good thresholds of all LDOs is checked 0.5ms after VCORE is enabled. If they are all OK, then there is a 11.5 ms delay and the MCU is released from reset. At this point, the MCU will begin executing instructions.

HVCP Power-up Sequence

The HVCP follows a typical power-up sequence as shown in Figure 5 below.

Figure 5 HVCP Power-up Sequence



The HVCP is enabled and disabled under firmware control in the PAC22140 when it is needed to drive the gates on the CHG and DSG FETs.

Hibernate Mode

The PAC22140 contains a very low-power mode that may be used to minimize power consumption from the battery when the battery monitor is not operating. Hibernate mode allows the device to enter an ultra-low-power mode where only critical circuitry is enabled. In this mode, only a minimal amount of current is used by VIN, and most of the Power Manager and all internal regulators are shut down to eliminate power drain from the output supplies. The user may enter hibernate mode by writing a register in the AFE.

Hibernate mode may be exited by three user selectable options

1) Push Button: by an active push-button input on the PB pin that is polarity selectable
2) PACK+ Charger Detect: by a PACK+ voltage selectable to 5V or 20V
3) Wakeup Timer: by the hibernate wakeup timer.

Power Monitoring

Whenever any of the VSYS, VCC33, VCCIO or VCORE power supplies falls below their respective power good threshold voltages, a fault event is detected and the MCU is reset. The MCU stays in the reset state until VSYS, VCC33, VCCIO and VCORE supply rails are all good again and the reset time has expired.

Power monitoring signals are provided onto the AFE MUX in the AFE for conversion by the 10-bit MCU ADC. The AFE MUX can select from the power monitoring signals: PACK+ * 0.02, BAT * 0.02, VIN * 0.02, VCORE, 0.4 * VCC33, 0.4 * VCCIO, 0.4 * VSYS, or VPTAT (temperature).

Temperature Monitoring

The device has monitoring for three junction temperatures. The MCU firmware can select whether to receive an interrupt when the device reaches any of the temperatures. Two temperatures, 120°C and 140°C, are warnings. A fault occurs when the junction temperature reaches 155°C and the MCU will be reset. The fault status bits are persistent during reset and can be read by the MCU upon re-initialization to determine the cause of the temperature fault reset.

Voltage References

There are two high-precision voltage references in the PAC22140: 2.5V and 0.5V.

The 2.5V high-precision reference is used by the MCU ADC (10-bit SAR), Voltage Sense ADC (16-bit Sigma-Delta) and AFE comparators. The 0.5V high-precision voltage reference is used by the Current Sense ADC (16-bit Sigma-Delta) and AFE comparators.

Electrical Characteristics

The Electrical Characteristics for the Power Manager are shown below.

HV-BUCK Electrical Characteristics

Table 1 HV-BUCK Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{norm}	VIN Normal mode supply current	Depending on Firmware Implementation and MCU clocking speed; No external loading.		5.5		mA
I_{sleep}	VIN Sleep mode supply current	CPU in deep sleep mode, systick clock disable, wait for interrupt. SCLK = CLKREF, turn off ROSC, turn off PLL, HCLK DIV = 8, all peripherals are disabled, CHG = OFF, DSG in Source Follower Mode, VCP = 0, No external loading		550		µA
$I_{HIB;VIN}$	VIN hibernate mode supply current	Hibernate mode active, VIN = 80V		3		µA
$V_{UVLOR;VIN}$	VIN UVLO rising threshold			19		V
$V_{UVLOF;VIN}$	VIN UVLO falling threshold			17		V
$V_{REF;VP}$	VP output regulation voltage		-5%	12	5%	V
$k_{POKR;VP}$	VP power OK threshold	VP rising		91		%
$k_{POKF;VP}$		VP falling		87		%
$k_{OVPR;VP}$	VP OV protection threshold	VP rising, blanking = 10µs		130		%
$t_{ONMIN;DRM}$	DRM minimum on time		90	200	300	ns
$t_{OFFMIN;DRM}$	DRM minimum off time		390	600	1150	ns
$V_{UVLOR;VP}$	VP UVLO rising			10		V
$V_{UVLOF;VP}$	VP UVLO falling			8		V
$V_{CSM;ILIM}$	CSM current limit threshold		-12%	0.2	12%	V
$F_{S;DRM}$	DRM switching frequency	Relative to switching frequency setting	-5		5	%
$I_{SOURCE;DRM}$	DRM output high source current			100		mA
$I_{SINK;DRM}$	DRM output low sink current			200		mA
	HV-BUCK inductor value			100		µH
$I_{DSG;HVBUCK}$	Discharge current			10		mA
V_{VIN}	HV-BUCK input voltage range		0		145	V
$V_{SRC;VSS}$	SRC to ground range		-10		VIN + 10	V
$V_{SRC;VIN}$	SRC to VIN range				10	V
$V_{BST;VSS}$	BST to ground range				145	V

VIN = 80V and T_A = -40°C to 105°C unless otherwise specified

HVCP Electrical Characteristics

Table 2 HVCP Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$I_{OP;VCP}$	VCP operating output current	Steady state; No external load				mA
$V_{OP;VCP}$	VCP operating voltage range	18V < BAT < 84V		BAT + 9		V
C_{VCP}	VCP capacitor value			0.47		µF
$V_{UVLOR;CP}$	Charge pump UVLO rising	Blanking = 100µs		BAT + 6		V
$V_{UVLOF;CP}$	Charge pump UVLO falling			BAT + 5		V

BAT = 80V and T_A = -40°C to 105°C unless otherwise specified

Linear Regulators Electrical Characteristics

Table 3 Linear Regulators Electrical Characteristics

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
V_{SYS}	VSYS output voltage	Total load up to 225mA		4.85	5.0	5.15	V
V_{CCIO}	VCCIO output voltage	Load = 10mA	VCCIO from regulator	3.152	3.3	3.398	V
			VCCIO shorted to VSYS		VSYS		V
V_{CC33}	VCC33 output voltage	Load = 10mA			3.3		V
V_{CORE}	VCORE output voltage	Load = 10mA			1.9		V
$I_{LIM;VSYS}$	VSYS regulator current limit			225	260		mA
$I_{LIM;VCCIO}$	VCCIO regulator current limit			90	130		mA
$I_{LIM;VCC33}$	VCC33 regulator current limit			40	57		mA
$I_{LIM;VCORE}$	VCORE regulator current limit			40	57		mA
k_{SCFB}	Short-circuit fold back				50		%
$V_{DO;VSYS}$	VSYS dropout voltage	VP = 12V, I_{VSYS} = 100mA			350	680	mV
$V_{UVLO;VSYS}$	VSYS UVLO threshold	VSYS rising, hysteresis = 0.2V		3.5	3.95	4.4	V
$k_{POK;VCCIO}$	VCCIO power OK threshold	VCCIO rising, hysteresis = 10%		85	90	95	%
$k_{POK;VCC33}$	VCC33 power OK threshold	VCC33 rising, hysteresis = 10%		85	90	95	%
$k_{POK;VCORE}$	VCORE power OK threshold	VCORE rising, hysteresis = 10%		85	90	95	%
C_{VSYS}	VSYS bypass capacitor value				4.7	10	µF
C_{VCC33}	VCC33 bypass capacitor value				2.2	10	µF
C_{VCORE}	VCORE bypass capacitor value				2.2	10	µF
C_{VCCIO}	VCCIO bypass capacitor value				2.2	10	µF

VIN = 80V and T_A = -40°C to 105°C unless otherwise specified

Power Monitor Electrical Characteristics

Table 4 Power Monitor Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{REF;25}$	Reference Voltage (2.5V)	T_A = 25°C	-0.5%	2.5	0.5%	V
		T_A = -40°C to 105°C		2.5		V
$V_{REF;05}$	Reference Voltage (0.5V)	T_A = 25°C	-0.5%	0.5	0.5%	V
		T_A = -40°C to 105°C		0.5		V
k_{MON}	Power Monitoring Voltage coefficient(1)	PACK+, BAT, VIN, VCP, CHG, DSG		0.02		V / V
		VCORE		1		V / V
		VSYS, VCCIO, VCC33	0.36	0.4	0.43	V / V
		VP, FUSE	0.09	0.1	0.11	V / V

VP = 12V and T_A = -40°C to 105°C unless otherwise specified

(1) The Power Monitoring Voltage Coefficient is the scale factor used to multiply the corresponding voltage to achieve the ADC input voltage range.

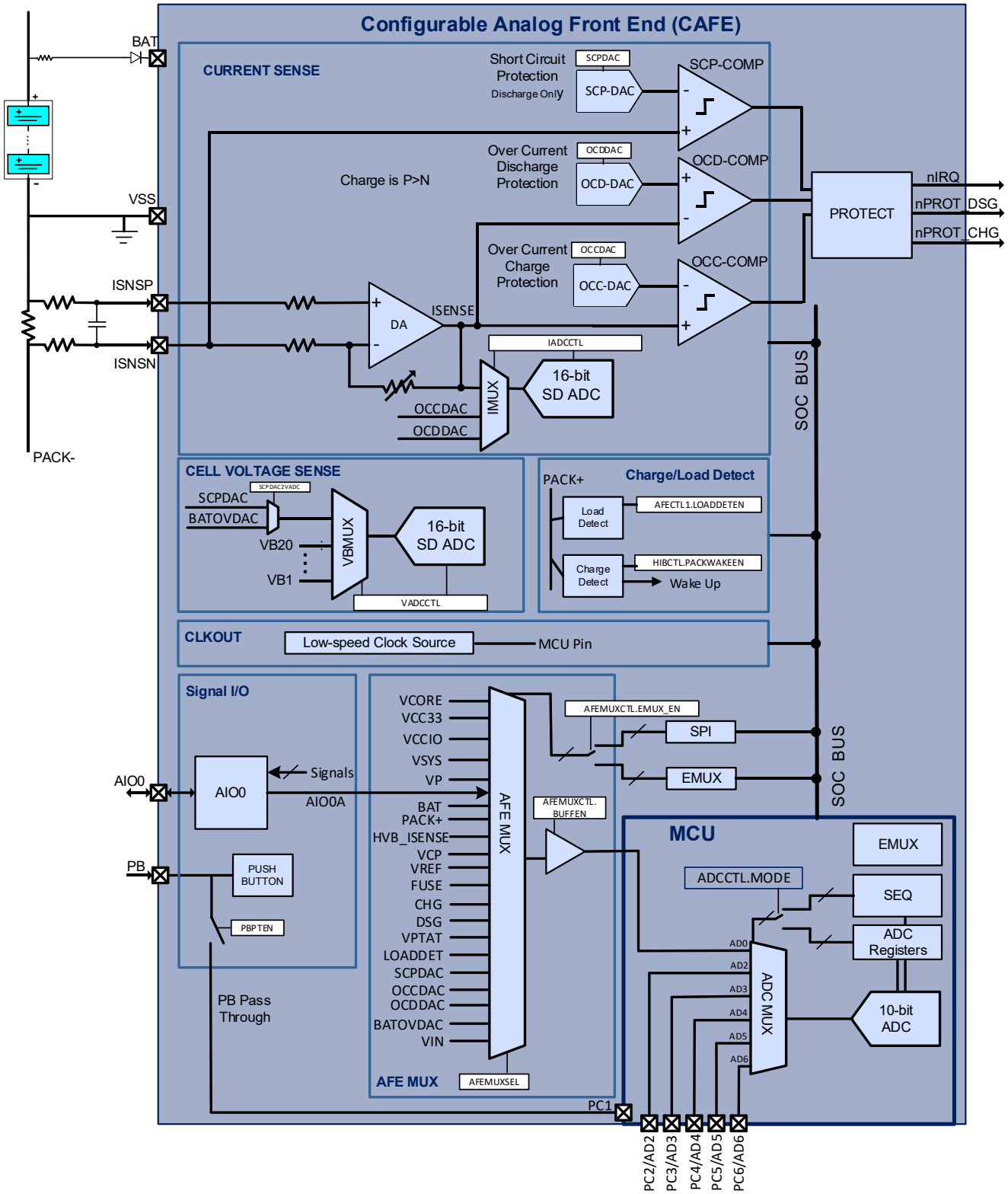
Configurable Analog Front-End (CAFE)

Features

- 16-bit Sigma-Delta ADC for current sense
- Current Sense Differential Programmable-Gain Amplifier
- Analog input/output gain amplifier with ADC Input or signal output selection
- Three comparators with DACs for programmable references for configurable OC warning or fault handling
- 16-bit Sigma-Delta ADC for Voltage Sampling of up to 20 cell voltages
- 12-bit Successive Approximation Register for Temperature sense and Pin ADC input and internal power supplies
- Internal Temperature warning and fault protection
- Push-Button (PB) input for exiting hibernate mode
- PACK+ Charge detection and Load detection
- 2kHz independent clock source

Block Diagram

Figure 6 CAFE Block Diagram



Functional Description

The PAC22140 contains a Configurable Analog Front-End (CAFE™) that can be used to sense battery pack current using an integrated Differential Amplifier (DA) and 16-bit Sigma-Delta ADC. The CAFE can configure three independent DACs to set three comparator thresholds for various programmable over-current detection for the battery pack.

The CAFE can also sense voltage and temperature internally through a MUX which contains inputs for each of the cell balance channels as well as the internal power supply rails from the power manager.

Current Sensing

The PAC22140 contains circuitry for battery pack current sense. The positive terminal (ISNSP) and negative terminal (ISNSN) are connected to each side of an external sense resistor. The ISNSP pin is connected to the positive terminal of a differential amplifier (DA) and the ISNSN pin is connected to the negative terminal of the amplifier. The differential amplifier has a programmable gain up to x128. This amplifier has a common-mode range of -0.3V to 0.5V. Using the gain stage allows a smaller current sense resistor, however, more noise will be introduced into the measurements.

The differential amplifier output is available for sampling from the 16-bit Current ADC.

To ensure accurate ADC conversion of the differential amplifier's output signal VISENSE * DAGAIN must remain within a voltage range of +/-0.5V. The current sense voltage VISENSE can be calculated using the following equation:

$$V_{ISENSE} = (ADC_{RESULT} * ADC_{GAIN} + ADC_{OFFSET}) / DA_{GAIN}$$

Where:

V_{ISENSE} is the voltage across the ISNSP and ISNSN pins.

ADC_{RESULT} is the 16-bit ADC result in counts

ADC_{GAIN} is 1.25V/216 counts = 19.073 µV/count

ADC_{OFFSET} is -0.625V

DA_{GAIN} is the selected differential amplifier gain

A theoretical ADC full scale reading of 0xFFFF equals 0.625V, a half scale reading of 0x8000 equals 0V, and 0x0000 = -0.625V.

To achieve the best accuracy, a calibration step should be performed after final assembly.

Over-Current Protection Comparators

There are three protection comparators that may be used for over-current protection: one for short circuit discharge protection (SCP-COMP), one for over-current discharge protection (OCD-COMP) and one for over-current charge protection (OCC-COMP) . The comparators have an operating range of 0 to 0.5V.

When one of the comparators trips, the device will send a signal to the driver manager, which can be programmed in various ways to disable the CHG/DSG FETs, as well as interrupt the MCU via an IRQ signal.

Over-Current Protection DACs

Each of the comparators has an 8-bit DAC that may be used to set the comparator reference. The DACs have an operating range of 0 to 0.5V.

Voltage Sensing

The PAC22140 also contains a 16-bit Sigma-Delta ADC that may be used for voltage sensing of the individual cells. A MUX selects from each of the individual cell balance nodes, VB1 to VB20, and one additional channel for SCPDAC or VBATOVDAC so that they may be sampled by the 16-bit ADC.

The MCU can use the SOC Bridge to access the MUX select, control the ADC operation, and read the 16-bit results.

AFE MUX

The CAFE also contains the AFE MUX that can be used to sample the internal power supply rails on the device, internal die temperature, and other signals.

The AFE MUX select can be controlled from the SOC bus or via the EMUX. The output of the AFE MUX is connected to the 10-bit ADC on the MCU so it may be sampled by the auto-sequencer.

The MUX channels that are available are:

- VCORE – 1.9V Core Logic LDO
- VCC33 – 3.3V Analog LDO
- VCCIO – 3.3V Digital I/O LDO
- VSYS – 5V System Supply
- VP – DC/DC Output
- HVB_ISENSE – High Voltage Buck Current Sense
- AIO0A – AIO0 Analog Output
- BAT – Battery Stack Input
- PACK+ - Charger Supply Input
- VCP – Charge Pump Output
- VREF – 2.5V Voltage reference
- FUSE – FUSE output
- CHG – CHG FET gate driver signal
- DSG – DSG FET gate driver signal
- VPTAT – Internal Temperature Sensor
- LOADDET – Load monitoring signal
- SCPDAC – Short Circuit Protection DAC output
- OCCDAC – Over Current Charge DAC output
- OCDDAC – Over Current Discharge DAC output
- BATOVDAC – Battery Over Voltage DAC output
- VIN – Main Input Supply Voltage

Temperature Monitoring and Protection

The PAC22140 has an integrated temperature sensor that is used for temperature warnings and faults and can also be sampled by the MCU ADC through the AFE MUX using the VPTAT MUX channel.

This value has a compensation coefficient available in INFO FLASH that can be used to obtain an accurate temperature. The parameter VT300K will be stored in INFO FLASH and will indicate the compensation factor.

The die temperature in degrees Kelvin can then be calculated by the following formula:

TKELVIN = 300 * (VPTAT + 0.075) / (VT300K + 0.075)

The PAC22140 contains two warning thresholds and one fault threshold:

- Warn 1: 120°C
- Warn 2: 140°C
- Fault: 155°C

If the internal temperature (VPTAT) rises above the Warn 1 threshold, the device will indicate this through a latched register bit. The user may enable a mask-able interrupt to the MCU to announce this condition.

If the internal temperature (VPTAT) rises above the Warn 2 threshold, the device will indicate this through a separate latched register bit. The user may enable an interrupt to the MCU to announce this condition. This will be the same interrupt as the Warn 1 threshold.

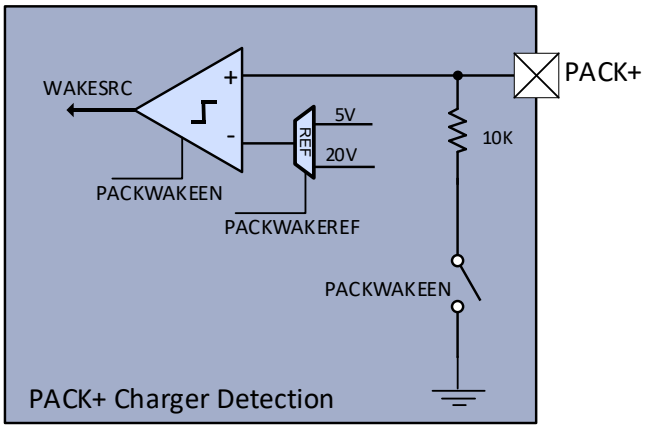
If the internal temperature (VPTAT) rises above the Fault threshold, the Charge pump, DC/DC and gate drivers will be disabled. The device will indicate this through a latched register bit. There is not interrupt for this condition. When the device falls below the temperature fault threshold, then the DC/DC will be re-enabled.

The temperature hysteresis level for all three thresholds is 10°C.

PACK+ Charger Detection

When properly configured the Pack+ Charger Detection can be used to exit hibernate mode. The threshold is selectable, and when PACK+ crosses it a wake up event occurs. To prevent PACK+ from floating a 10kΩ can be enabled to pull PACK+ low.

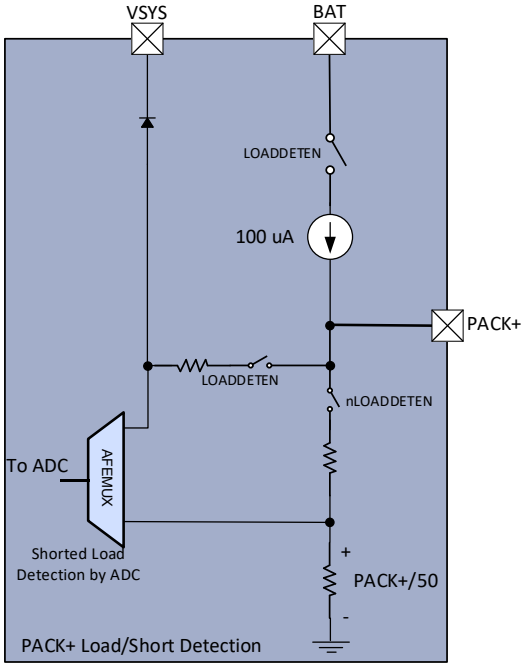
Figure 7 PACK+ Charger Detection



PACK+ Load/Short Detection

When properly configured the load detection can be used for load or shorted load event detection. This requires firmware to move the state of the system into the proper configuration. Either a load or a shorted load can be detected. This detection is disabled during hibernate mode.

Figure 8 PACK+ Load/Short Detection



Push-Button (PB) Input

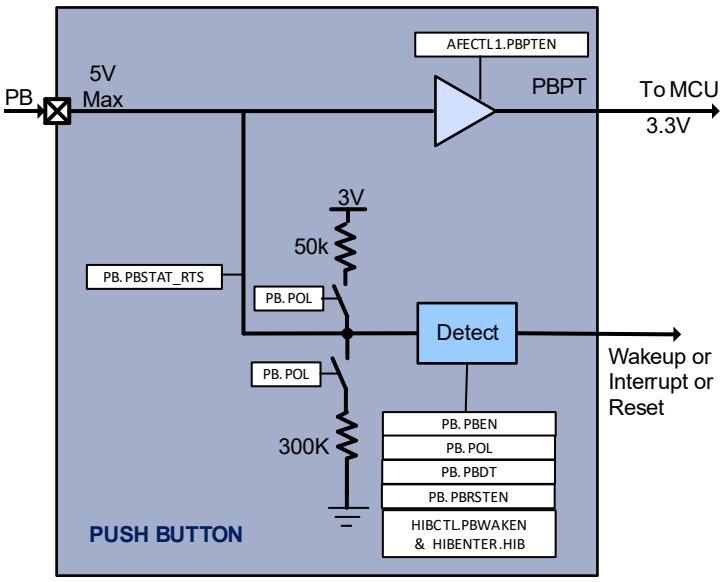
The PAC22140 contains a push-button input pin (PB) and a push-button module (see Figure 9 below). A push-button pass through to the MCU can be enabled so that the MCU can read the state of the digital PB pin directly on the PC1 GPIO.

The push-button module can be used to wake-up the device from hibernate, interrupt the MCU, or reset the device. The push-button polarity can be set to active high or active low using the polarity setting.

The push-button module can be configured so that an active PB will wake up the PAC22140 from hibernate mode.

When enabled, the push-button may also be used as a hardware reset when held active for longer than 8s during normal operation. Once the push-button is enabled, the polarity setting will determine whether the PB input will be pulled up to 3V with a 50kΩ resistor or pulled down to GND with a 300kΩ resistor. There is also a programmable de-glitch time that may be configured to 1, 4, 8, or 32ms.

Figure 9 Push-Button (PB) Input



Low-speed Clock Source

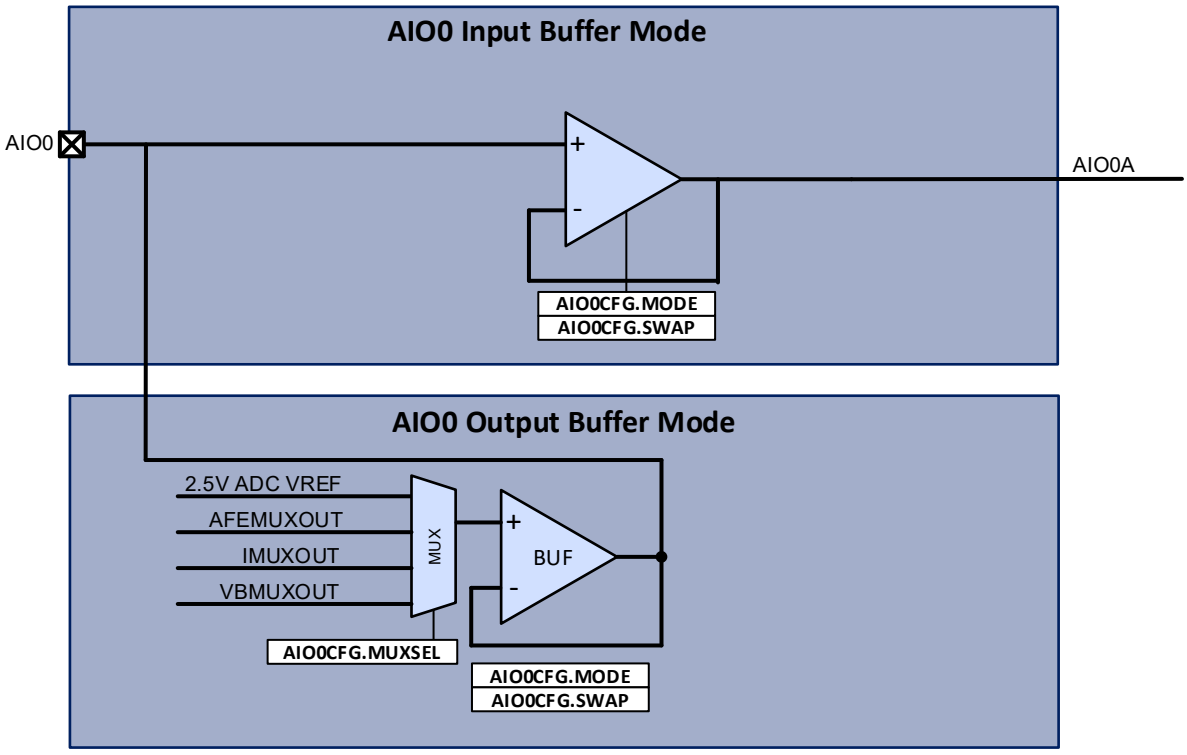
The PAC22140 contains a configurable frequency low-speed independent clock source that can be used for applications that require Class B safety requirements. This clock source may be configured from 500Hz to 2kHz and its output is connected to the PA5 GPIO input on the MCU.

AIO0 – Analog Input Output

The PAC22140 has an AIO0 module and pin that includes a buffer for analog I/O (see Figure 10 below). The AIO0 pin can be configured as an input where the output of the buffer AIO0A is routed to the AFE Mux for input to the MCU ADC. Or, the AIO0 pin can be configured to output internal signals of the AFE. The following signals are available for output on the AIO0 pin:

- VREF – 2.5V Voltage Reference
- AFEMUXOUT – AFE Mux Output to the MCU ADC
- IMUXOUT – Current Mux Output to the Current ADC
- VBMUXOUT – Battery Cell Voltage Mux Output to the Voltage ADC

Figure 10 AIO0 Analog Input Output



Electrical Characteristics

The Electrical Characteristics for the CAFE are shown below.

Differential Amplifier (DA) Electrical Characteristics

Table 5 DA Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{ICMR;DA}$	Input common mode range		-0.3		0.5	V
$V_{OLR;DA}$	Output linear range		0.1		VSYS – 0.1	V
$I_{CC;DA}$	Operating supply current			150		µA
$V_{OS;DA}$	Input offset voltage	Gain = 8x	-8		8	mV
$k_{CMRR;DA}$	Common mode rejection ratio		50	80		dB
$R_{INDIF;DA}$	Differential input impedance			80		kΩ
$A_{VZI;DA}$	Amplifier gain(1)	Gain = 1x		1		
		Gain = 2x		2		
		Gain = 4x		4		
		Gain = 8x, V_{DAxP}=V_{DAxN}=0V, T_A = 25°C	-2	8	2	%
		Gain = 16x		16		
		Gain = 32x		32		
		Gain = 64x		64		
		Gain = 128x		128		

(1) For proper ADC conversion and Over-Current protection, V_{ISENSE} * DA_{GAIN} must be within +/- 0.5V

T_A = -40°C to 105°C unless otherwise specified

Current Sense ADC Electrical Characteristics

Table 6 Current Sense ADC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{ADCONV;ADC16}$	ADC conversion time			1.5		ms
	ADC resolution			16		bits
	ADC effective resolution		15			bits
	ADC differential non-linearity (DNL)			+/- 0.5		LSB
	ADC integral non-linearity (INL)			+/- 6	+/- 20	LSB
	ADC offset error	Ta=25°C, Diff. Amp. Gain x1, after applying calibration factors		130		µV
	ADC gain error	Ta=25°C, Diff. Amp. Gain x1, after applying calibration factors		1.25		%FS

T_A = -40°C to 105°C unless otherwise specified

Short Circuit Protection Comparator (SCP-COMP) Electrical Characteristics

Table 7 SCP-COMP Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$I_{CC;\ SCP\text{-}COMP}$	Operating supply current			10		µA
$V_{ICMR;\ SCP\text{-}COMP}$	Input range	Relative to common mode voltage	0		0.5	V
$V_{OS;\ SCP\text{-}COMP}$	Input offset voltage	T_A=25°C	-10		10	mV
$V_{HYS;\ SCP\text{-}COMP}$	Hysteresis			50		mV
$t_{DT;\ SCP\text{-}COMP}$	Comparator deglitch time	10mV difference input		1		µs

T_A = -40°C to 105°C unless otherwise specified.

Over-Current Discharge Protection Comparator (OCD-COMP) Electrical Characteristics

Table 8 OCD-COMP Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$I_{CC;\ OCD\text{-}COMP}$	Operating supply current			10		µA
$V_{ICMR;\ OCD\text{-}COMP}$	Input range	Relative to common mode voltage	0		0.5	V
$V_{OS;\ OCD\text{-}COMP}$	Input offset voltage	T_A=25°C	-10		10	mV
$V_{HYS;\ OCD\text{-}COMP}$	Hysteresis			50		mV
$t_{DT;\ OCD\text{-}COMP}$	Comparator deglitch time	10mV difference input		10		µs

T_A = -40°C to 105°C unless otherwise specified.

Over-Current Charge Protection Comparator (OCC-COMP) Electrical Characteristics

Table 9 OCC-COMP Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$I_{CC;\ OCC\text{-}COMP}$	Operating supply current			10		µA
$V_{ICMR;\ OCC\text{-}COMP}$	Input range	Relative to common mode voltage	0		0.5	V
$V_{OS;\ OCC\text{-}COMP}$	Input offset voltage	T_A=25°C	-10		10	mV
$V_{HYS;\ OCC\text{-}COMP}$	Hysteresis			50		mV
$t_{DT;\ OCC\text{-}COMP}$	Comparator deglitch time	10mV difference input		10		µs

T_A = -40°C to 105°C unless otherwise specified.

Voltage ADC

Each of the battery cell voltages are available for sampling from the 16-bit Voltage ADC. The ADC was designed to accurately convert voltages between 1.8V and 4.7V. The Voltage ADC equation is given by:

$V_{CELL} = ADC_{RESULT} * ADC_{GAIN} + ADC_{OFFSET}$

Where:

V_{CELL} is the voltage of the converted cell

ADC_{RESULT} is the ADC result in counts

ADC_{GAIN} is $12.5V/2^{16}$ counts = 190.73 µV/count

ADC_{OFFSET} is -6.25V.

A theoretical ADC full scale reading of 0xFFFF equals 6.25V and a half scale reading of 0x8000 equals 0V.

Cell Voltage ADC Electrical Characteristics

Table 10 Cell Voltage ADC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
$t_{ADCONV;ADC16}$	ADC conversion time	f_{ADCLK} = 16MHz		5		ms
	ADC resolution			16		bits
	ADC effective resolution		14			bits
	ADC differential non-linearity (DNL)			+/- 0.3		LSB
	ADC integral non-linearity (INL)			+/- 4		LSB
	ADC offset error	Ta=25°C after calibration		3		LSB
	ADC gain error	Ta=25°C after calibration		0.82		%FS

TA = -40°C to 105°C unless otherwise specified

Cell Voltage Measurement Accuracy Electrical Characteristics

Table 11 Cell Voltage Measurement Accuracy Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
$V_{CELL;ACC}$	Cell voltage measurement accuracy (1)	3.2V <= Vcell <= 4.2V; 1.8V <= Vcell <= 4.7V; T_A = 25°C;(1)		+/-2.5 +/-5		mV
		3.2V <= Vcell <= 4.2V; 1.8V <= Vcell <= 4.7V; T_A = 0°C to 85°C;(1)	-10 -15		10 15	mV
		3.2V <= Vcell <= 4.2V; 1.8V <= Vcell <= 4.7V; TA = -40°C to 105°C;(1)	-20 -30		20 30	mV

(1) After ADC Calibration

TA = -40°C to 105°C unless otherwise specified

Push-Button Electrical Characteristics

Table 12 Push-Button Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
$V_{I,PBTN}$	Input voltage range		0		5	V
$V_{IH,PBTN}$	High-level input voltage		2.2			V
$V_{IL,PBTN}$	Low-level input voltage				1.4	V
$R_{PU;PBTN}$	Pull-up resistance	To 3V, push-button enabled PB.POL = Active Low		50		kΩ
$R_{PD;PBTN}$	Pull-down resistance	To GND, push-button enabled PB.PBPOL = Active high		300		kΩ

T_A = -40°C to 105°C unless otherwise specified

Temperature Protection Electrical Characteristics

Table 13 Temperature Protection Electrical Characteristics

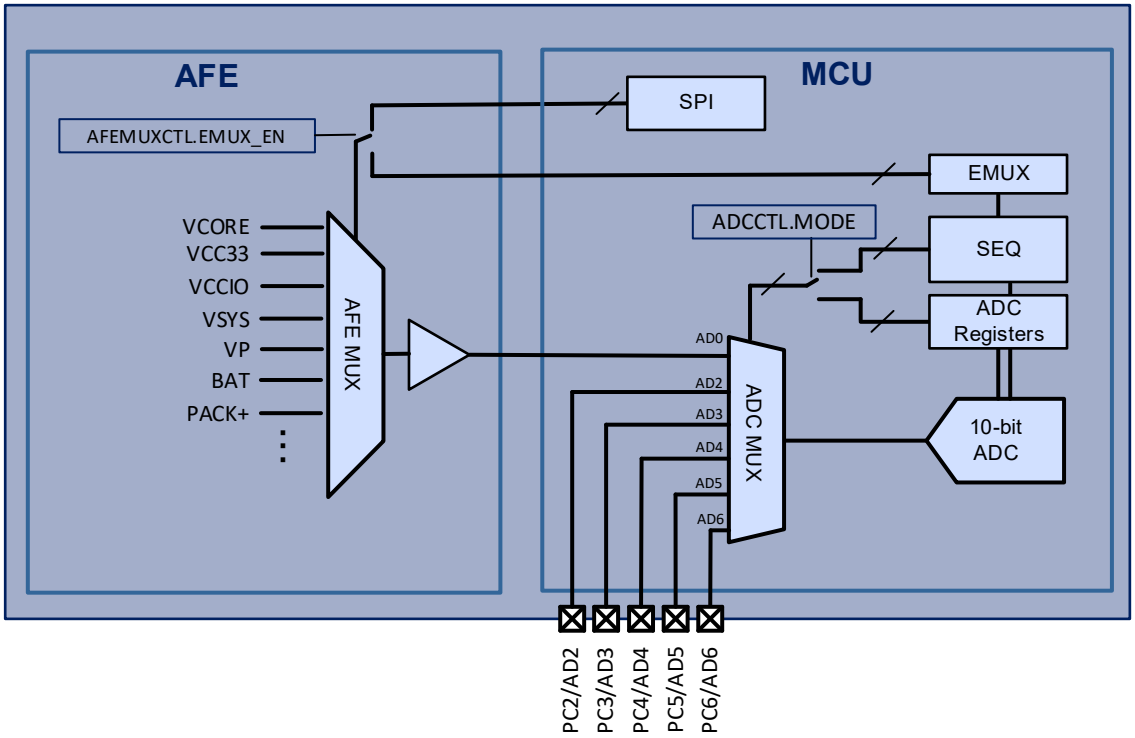
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
T_{WARN1}	Temperature warning 1 threshold			120		ºC
$T_{WARN1;HYS}$	Temperature warning 1 hysteresis			10		ºC
$T_{WARN1;BLANK}$	Temperature warning 1 blanking			10		µs
T_{WARN2}	Temperature warning 2 threshold			140		ºC
$T_{WARN2;HYS}$	Temperature warning 2 hysteresis			10		ºC
$T_{WARN2;BLANK}$	Temperature warning 2 blanking			10		µs
T_{FAULT}	Temperature fault threshold			155		ºC
$T_{FAULT;HYS}$	Temperature fault hysteresis			10		ºC
$T_{FAULT;BLANK}$	Temperature fault blanking			10		µs

T_A = -40°C to 105°C unless otherwise specified

10-bit ADC With Auto-Sampling Sequencer

Block Diagram

Figure 11 10-bit MCU ADC Block Diagram



Functional Description

ADC

The analog-to-digital converter (ADC) is a 10-bit successive approximation register (SAR) ADC with 1 µs conversion time and up to 1MSPS capability. The ADC input clock has a user-configurable divider from /1 to /8 of the system clock. The integrated analog multiplexer allows selection from up to 5 direct ADx inputs via the Port C pins, or several internally sampled voltages in the Configurable Analog Front End (CAFE). The ADC can be configured for repeating or non-repeating conversions and can interrupt the microcontroller when a conversion is finished.

Auto-Sampling Sequencer

Two independent and flexible auto-sampling sequencer state machines allow signal sampling using the ADC without interaction from microcontroller core. Each auto-sampling sequencer state machine can be programmed to take and store up to 8 samples each in the ADC result register from different analog inputs, able to control the ADC MUX and AFE MUX. The sampling start of the auto-sampling sequencer can be precisely triggered using timers A, B, C, or D or any of their associated PWM edges (high-to-low or low-to-high). It also supports manual start or a ping-pong-scheme, where one auto-sampling sequencer state machine triggers the other when it finishes sampling.

The auto-sampling sequencer can interrupt the microcontroller when either conversion sequence is finished.

EMUX Control

A dedicated low latency interface controllable by the auto-sampling sequencer or register control allows changing the ADC MUX and AFE MUX, allowing back to back conversions of multiple analog inputs without microcontroller interaction.

Electrical Characteristics

Table 14 10-bit MCU ADC and Auto-Sampling Sequencer Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
ADC						
f_{ADCLK}	ADC conversion clock input				16	MHz
t_{ADCONV}	ADC conversion time	f_{ADCLK} = 16MHz			1	µs
	ADC resolution			10		bits
	ADC effective resolution		9.2			bits
	ADC differential non-linearity (DNL)			±0.5		LSB
	ADC integral non-linearity (INL)			±1		LSB
	ADC offset error			0.6		%FS
	ADC gain error			0.12		%FS
Reference Voltage						
V_{REFADC}	ADC reference voltage input			2.5		V
Sample and Hold						
t_{ADCSH}	ADC sample and hold time	f_{ADCLK} = 16MHz		188		ns
C_{ADCIC}	ADC input capacitance			1.3		pF
Input Voltage Range						
V_{ADCIN}	ADC input voltage range	ADC multiplexer input	0		V_{REFADC}	V
EMUX Clock Speed						
$f_{EMUXCLK}$	EMUX engine clock input				50	MHz

V_{SYS} = V_{CCIO} = 5V, V_{CC33} = 3.3V, V_{CC18} = 1.8V, and T_A = -40°C to 105°C unless otherwise specified

Application Specific Power Drivers (ASPD)

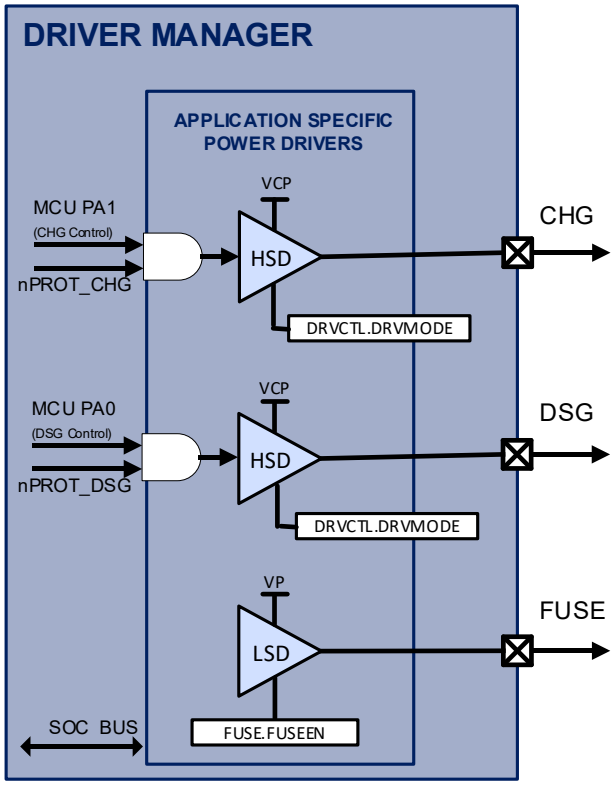
Gate Drivers

Features

- High-Side gate drivers for CHG and DSG FET
- Low-side gate driver for external FUSE

Block Diagram

Figure 12 ASPD Block Diagram



- Functional Description

The Application Specific Power Drivers™ (ASPD) module drives the gate of the external CHG and DSG FETs and external protection fuse FET for the battery pack.

The CHG and DSG FET gates are driven from the CHG and DSG pins. The typical gate drive ON voltage for the CHG and DSG FETs is VCP (BAT + 9V). Source Follower Mode can be selected for lower current operations and not require enabling the charge pump. In this mode, CHG drive is off and DSG is on with a pull up to BAT. The mode is control by the DRVMODE control bits (see Users Guide). Protection mechanisms from the battery over voltage and over current comparators will also be applied as configured in the AFE protection registers. Once the CHG and DSG gate drivers enable bits are set in the analog front end (AFE), the MCU must also set the appropriate GPIOs to drive the gate driver outputs high/ON.

The FUSE output is a low-side switch supplied by VP which is intended for driving the gate on an external FET which is typically used to below an external fuse in series with PACK+ and the battery stack. The FUSE can support other low-side driver needs such as driving an LED..

Electrical Characteristics

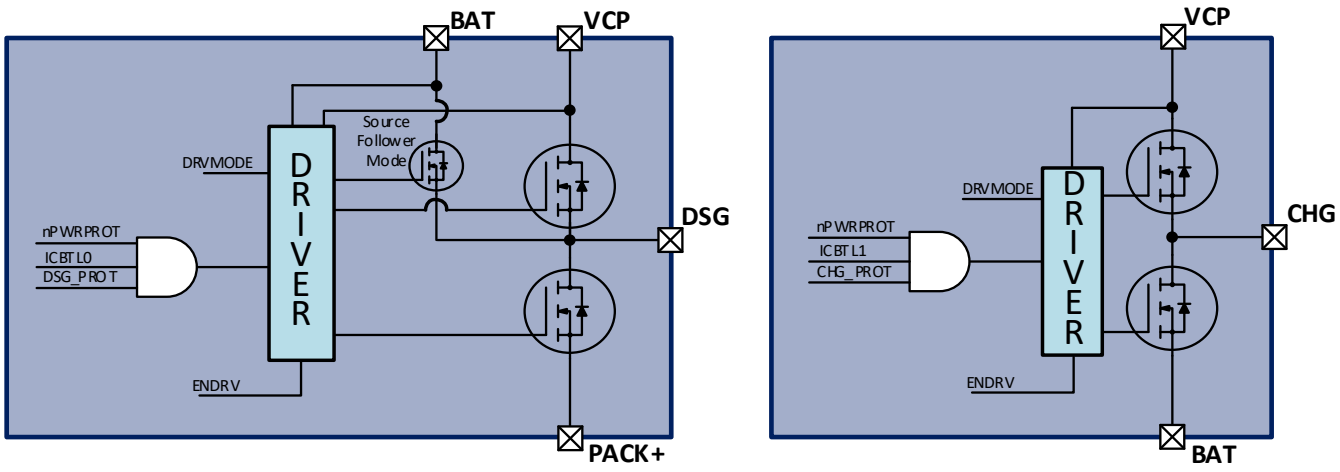
The Electrical Characteristics for the ASPD are shown below.

Table 15 ASPD Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
V_{FETON}	CHG or DSG FET On with respect to BAT	CHG/DSG C_L = 20 nF		9		V
$V_{CHGFETOFF}$	CHG FET Off (with respect to BAT)	CHG/DSG C_L = 20 nF			0.3	V
$V_{DSGFETOFF}$	DSG FET Off (with respect to PACK+)	CHG/DSG C_L = 20 nF			0.3	V
$V_{SRCFLWR}$	DSG on voltage (with respect to BAT)	CHG/DSG C_L = 20 nF		0		V
$t_{FETrise}$	CHG or DSG rise time 0.3V to 5V (with respect to BAT)	CHG/DSG C_L = 20 nF, R_{GATE} = 100 Ω		10	20	µs
$t_{CHGFETfall}$	CHG FET fall time to BAT + 0.3V	CHG/DSG C_L = 20 nF, R_{GATE} = 100 Ω		15	30	µs
$t_{DSGFETfall}$	DSG FET fall time to PACK+ + 0.3V	CHG/DSG C_L = 20 nF, R_{GATE} = 100 Ω		15	30	µs
V_{FUSE}	FUSE High Voltage	C_L = 1nF Assumes valid VIN		Vp		V
$t_{FUSErise}$	FUSE rise time	C_L = 1nF Time to 90% of V_{FUSE}		0.5		µs
$R_{FUSEdriver}$	FUSE driver output resistance			200		Ω

T_A = -40°C to 105°C unless otherwise specified

Figure 13 High Side Gate Drivers



Integrated Cell Balancing

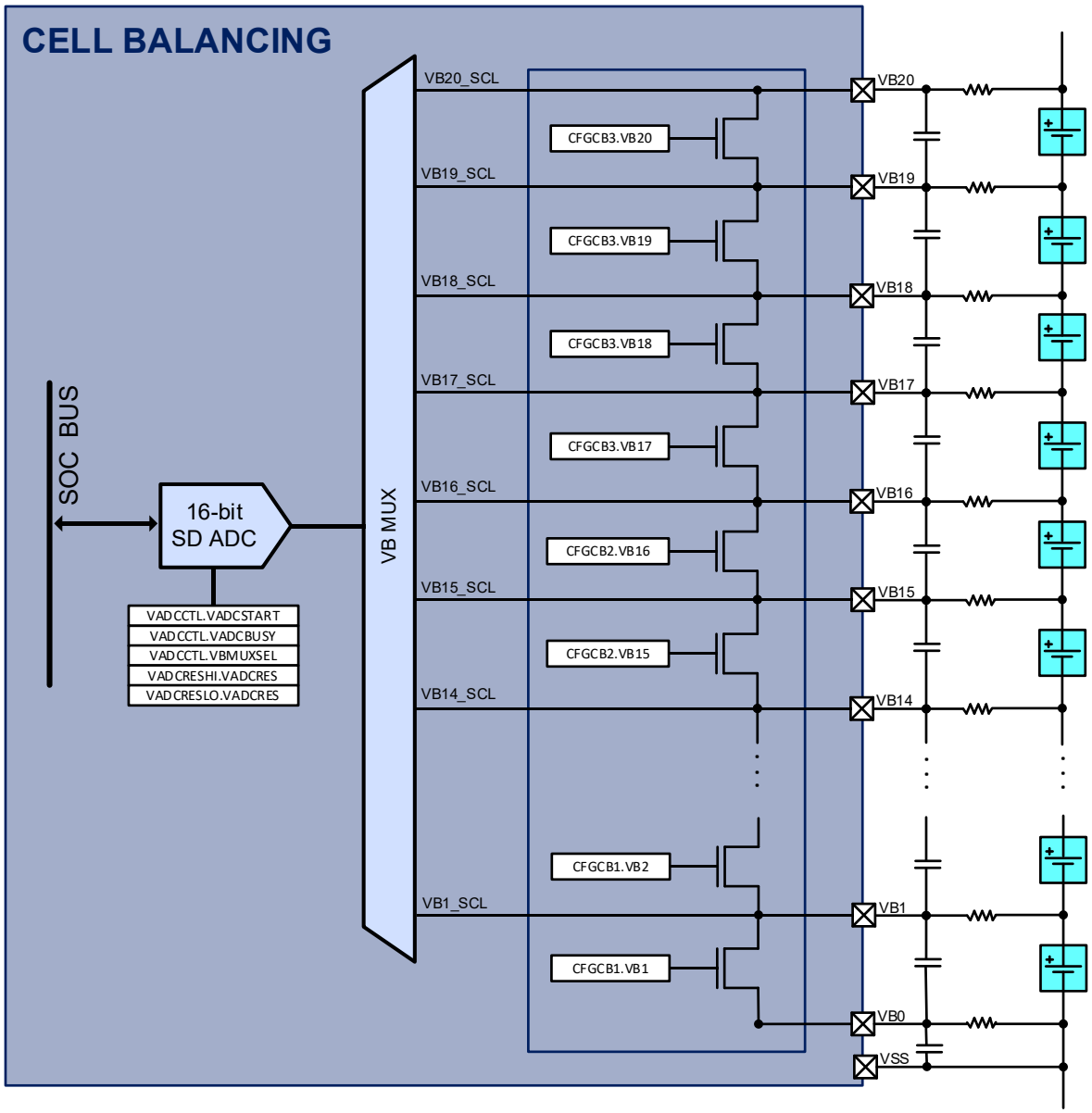
The PAC22140 contains integrated cell balancing FETs for up to 20 cells.

Features

- FETs for each cell to allow discharge of individual cells
- Voltage ADC for sensing the voltage of each cell

Block Diagram

Figure 14 Cell Balancing



- Cell Balancing FETs

The integrated cell balancing contains FETs for up to 20 battery cells. Cell balancing can be performed through firmware programming.

Adjacent cells should not be balanced at the same time. In the event that too many cells are being balanced at the same time and Thermal protection occurs, then the cell balancing will be shut down first.

The Electrical Characteristics for the Cell Balancing are shown below.

Table 16 Cell Balancing Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
	Number of cells		10		20	cells
V_{VB}	Cell voltage range		1.8	3.6	4.7	V
I_{VB}	Cell balance output current	V_{VB} = 4.2V		50		mA
$R_{DS(ON);CB}$	Cell balance FET $R_{DS(ON)}$	1.8V <= Vcell <= 4.7V		25		Ω
	External cell balance resistors		20	30		Ω

T_A = -40°C to 105°C unless otherwise specified

Battery AFE Windowed Watchdog Timer (WWDT)

This section describes the requirements for the BMS AFE Windowed Watchdog Timer (WWDT) module.

The SOC Bus Windowed Watchdog Timer must be accessed over the SOC Bridge I/F and can be used to reset the entire device if not reset at periodic intervals.

Wake-up Timer

The wake-up timer can be used for very low power hibernate and sleep modes to wake up the device periodically. It can be configured to be 125ms, 250ms, 500ms, 1s, 2s, 4, or 8s.

This AFE WWDT provides greater flexibility than previous AFE WDTs such that customers have a better chance of matching the WDT time to their system requirements. Using the AFE WWDT will provide a more complete device reset than the digital WDT.

The Windowing feature gives better robustness against rogue software that might be in a loop resetting the WDT continuously.

To comply with safety requirements, the WWDT shall be clocked from the 32 kHz Oscillator and not the 4 MHz CLKREF.

When the WWDT issues a reset, a Flag bit shall be set in the AFE reset status register indicating the WWDT caused the reset. Register bits shall be reset or retained per the Reset column in the Register Map (see Users Guide)

A key benefit of the AFE WWDT is that it will reset the MCU and also the majority of the battery AFE.

Figure 15 WWDT System Block Diagrams

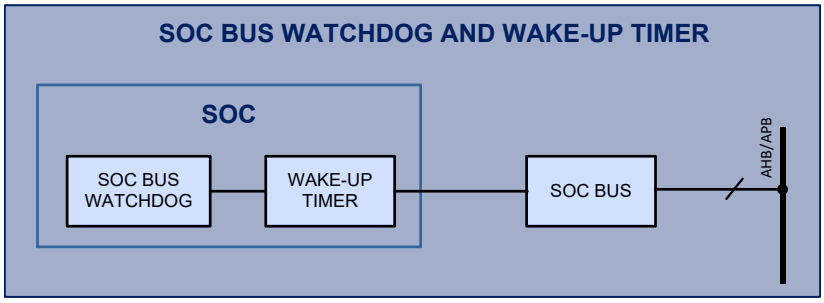
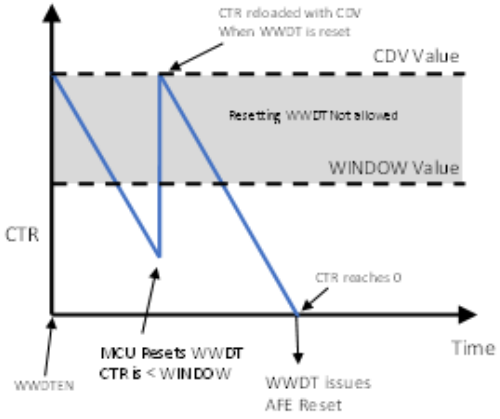
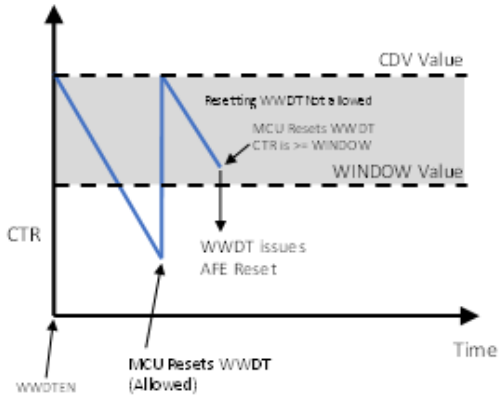


Figure 16 WWDT Operation



Normal MCU Resetting of the WWDT and CTR reaches 0



MCU Resets WWDT when CTR is > WINDOW value

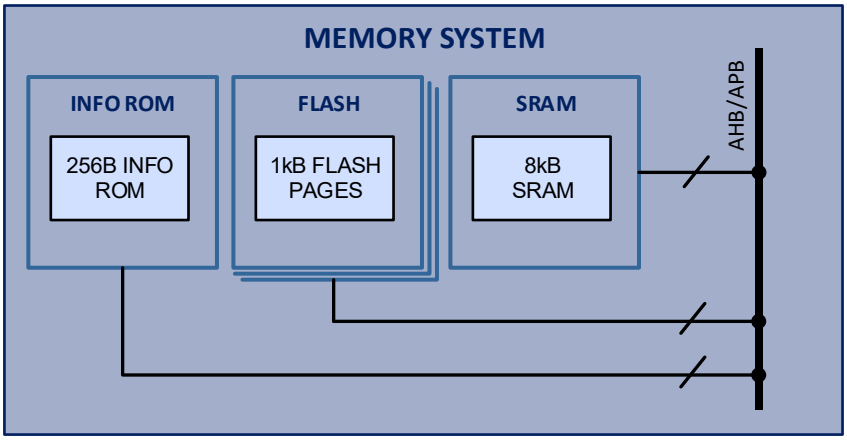
Memory System

Features

- 32kB embedded FLASH
  - 100,000 program/erase cycles
  - 10 years data retention
- 256B INFO- embedded FLASH
  - Data storage, configuration, or parameter storage
- 8kB SRAM

Block Diagram

Figure 17 Memory System Block Diagram



Functional Description

The device has multiple banks of embedded FLASH memory, SRAM memory, as well as peripheral control registers that are all program-accessible in a flat memory map.

Program and Data FLASH

32kB in 32 pages of 1kB each is available for program or data memory. Each of them can be individually erased or written to while the microcontroller is executing a program from SRAM.

INFO FLASH

The PAC22140 Memory Controller provides access to the INFO FLASH memories, a 256B page which is a Read-only memory that contains device-specific information such as the device ID, a unique ID, trimming and calibration data that may be used by programs executing on the PAC22140.

SRAM

Up to 8kB contiguous array of SRAM is available for non-persistent data storage. The SRAM memory supports word (4-byte), half-word (2-byte) and byte address aligned access. The microcontroller may execute code out of SRAM for time-critical applications, or when modifying the contents of FLASH memory.

Electrical Characteristics

Table 17 Memory System Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Embedded FLASH						
$t_{READ;FLASH}$	FLASH read time		40			ns
$t_{WRITE;FLASH}$	FLASH write time		20			µs
$t_{PERASE;FLASH}$	FLASH page erase time				10	ms
$N_{PERASE;FLASH}$	FLASH program/erase cycles			100k		cycles
$t_{DR;FLASH}$	FLASH data retention		10			years
SRAM						
t_{SRAM}	SRAM access cycle time		20			ns

(V_{SYS} = V_{CCIO} = 5V, V_{CC33} = 3.3V, V_{CC18} = 1.8V, and T_A = -40°C to 105°C unless otherwise specified.)

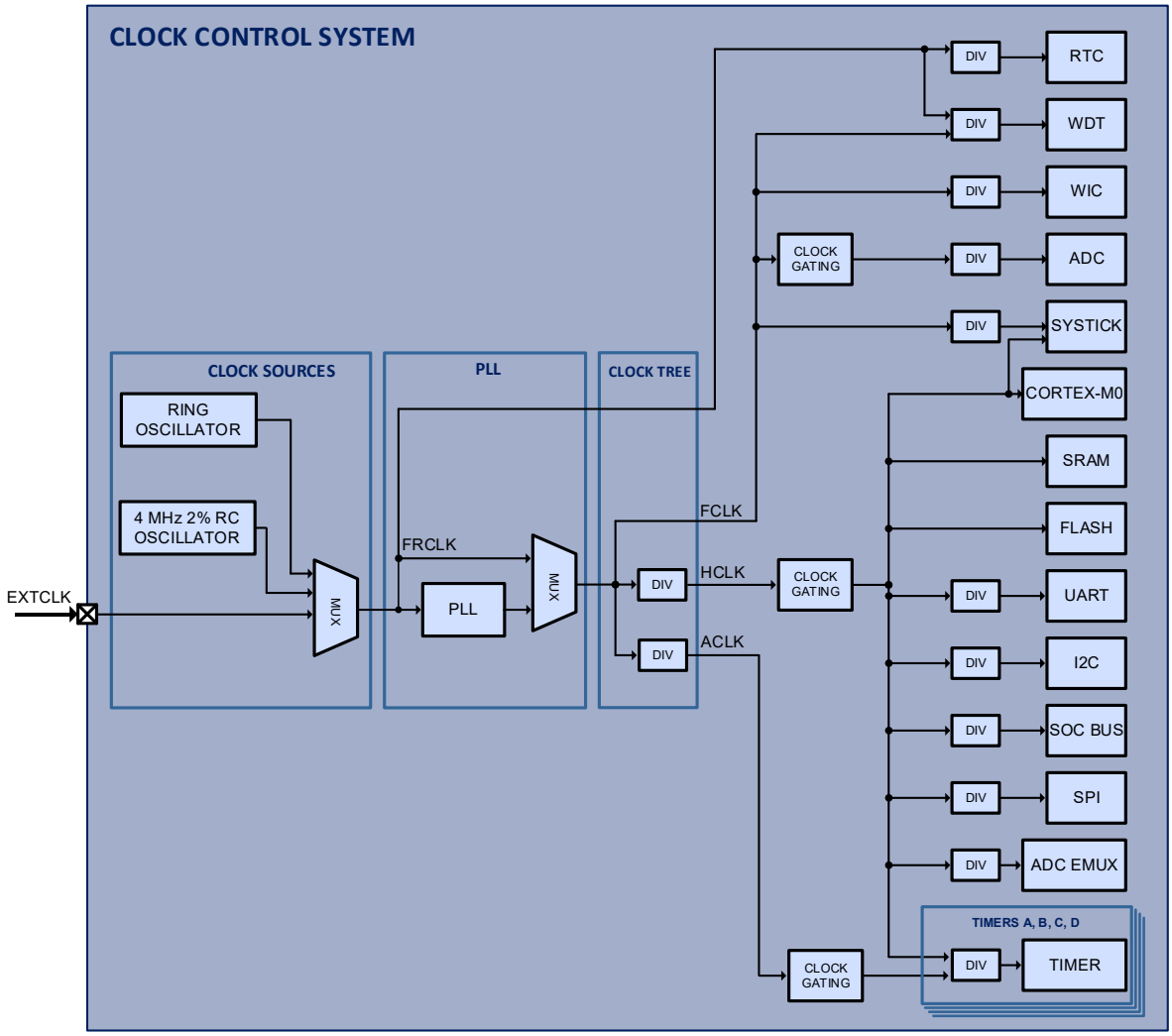
Clock Control System

Features

- Ring oscillator with 7.5MHz, 9.6MHz, 13.8MHz, and 25.7MHz settings
- High accuracy 2% trimmed 4MHz RC oscillator
- External clock input up to 40MHz
- PLL with 1MHz to 25 MHz input, and 3.5MHz to 100MHz output
- /1 to /8 clock divider for HCLK
- /1 to /128 clock divider for ACLK

Block Diagram

Figure 18 CCS Block Diagram



Functional Description

The PAC clock control system covers a wide range of applications.

Free Running Clock (FRCLK)

The free running clock (FRCLK) is generated from one of the 4 clock sources: ring oscillator, trimmed RC oscillator, crystal driver or external clock input. The FRCLK is used for the real-time clock (RTC), watchdog timer (WDT), input to the PLL, or FCLK source to clock the system in low power and sleep mode.

Fast Clock (FCLK)

The fast clock (FCLK) is generated from the PLL or supplied by the FRCLK directly. The FCLK supplies the watchdog timer (WDT), ADC, wake-up interrupt controller (WIC), SysTick timer, Arm® Cortex®-M0 peripheral high speed clock (HCLK) and low speed clock (LSCLK).

High-Speed Clock (HCLK)

The high-speed clock (HCLK) is derived from the FCLK with a /1, /2, /4 or /8 divider. It supplies the peripheral AHB/APB bus, Timers A to D, dead-time controllers, SPI interface, I^2C interface, UART interface, EMUX interface, SOC bus bridge and memory subsystem, and can go as high as 50MHz.

Auxiliary Clock (ACLK)

The auxiliary clock (ACLK) is derived from FCLK with a /1, /2, to /128 divider, and supplies the timer and dead-time blocks. It can be clocked faster or slower than HCLK and can go as high as 100MHz.

Clock Gating

The clock tree supports clock gating in deep-sleep mode for the timer block, ADC, SPI interface, I^2C interface, UART interface, memory subsystem and the Arm® Cortex®-M0 itself.

Ring Oscillator (ROSC)

The integrated ring oscillator provides 4 different clocks with 7.5MHz, 9.6MHz, 13.8MHz, and 25.7MHz settings. After reset, the clock tree always defaults to this clock input with the lowest frequency setting.

Trimmed 4MHz RC Oscillator

The 2% trimmed 4MHz RC oscillator provides an accurate clock suitable for many applications. It is also used to derive the clock for the Multi-Mode Power Manager.

Internal Slow RC Oscillator

An internal 32kHz RC oscillator is used during start up to provide an initial clock to analog circuitry. It is not used as a clock input to the clock tree.

External Clock Input

The clock tree can be supplied with an external clock up to 40MHz.

PLL

The integrated PLL input clock is supplied by the FRCLK with an input frequency range of 1MHz to 25MHz. The PLL output frequency is adjustable from 3.5MHz to 100MHz.

Electrical Characteristics

Table 18 CCS Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Clock Tree (FRCLK, FCLK, HCLK and ACLK)						
f_{FRCLK}	Free-running clock frequency				50	MHz
f_{FCLK}	Fast clock frequency				100	
f_{HCLK}	High-speed clock frequency				100	
f_{ACLK}	Auxilliary clock frequency				100	
Internal Oscillators						
f_{ROSC}	Ring oscillator frequency	Frequency setting = 11b		7.5		MHz
		Frequency setting = 10b		9.6		
		Frequency setting = 01b		13.8		
		Frequency setting = 00b		25.7		
f_{TRIM}	Trimmed RC oscillator frequency	TA = 25°C	-2%	4	2%	MHz/%
		TA = -40°C to 105°C	-3%	4	3%	
	Trimmed RC oscillator clock jitter	TA = -40°C to 85°C		0.5		%
External Clock Input						
f_{EXTCLK}	External clock input frequency range				40	MHz
$t_{HIGH;EXTCLK}$	External clock high time		10			ns
$t_{LOW;EXTCLK}$	External clock low time		10			ns
PLL						
f_{INPLL}	PLL input frequency range		2		25	MHz
f_{OUTPLL}	PLL output frequency range		3.5		100	MHz
	PLL settling time			0.5		ms
	PLL period jitter	RMS		30		ps
		Peak to peak		±150		

(V_{SYS} = V_{CCIO} = 5V, V_{CC33} = 3.3V, V_{CC18} = 1.8V, and T_A = -40°C to 105°C unless otherwise specified.)

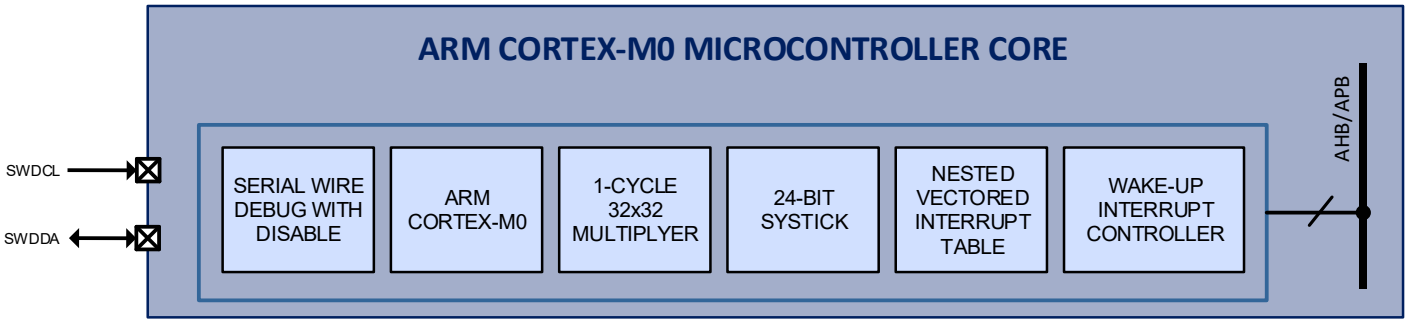
Arm® CORTEX®-M0 Microcontroller Core

Features

- Arm® Cortex®-M0 core
- Fast single-cycle 32-bit x 32-bit multiplier
- 24-bit SysTick timer
- Up to 50MHz operation
- Serial wire debug (SWD), with 4 breakpoint and 2 watch-point unit comparators
- Nested vectored interrupt controller (NVIC) with 25 external interrupts
- Wake-up interrupt controller (WIC) with GPIO, real-time clock (RTC) and watchdog timer (WDT) interrupts enabled
- Sleep and deep-sleep mode with clock gating

Block Diagram

Figure 19 Arm® Cortex®-M0 Microcontroller Core Block Diagram



Functional Description

The Arm® Cortex®-M0 microcontroller core is configured for little endian operation and includes the fast single-cycle 32-bit multiplier and 24-bit SysTick timer and can operate at a frequency of up to 50MHz.

The microcontroller nested vectored interrupt controller (NVIC) supports 25 external interrupts for the device's peripherals and sub-systems. For low-latency interrupt processing, the NVIC also supports interrupt tail-chaining. The wake-up interrupt controller (WIC) can wake up the device from low-power modes using any GPIO interrupt, as well as from the RTC or WDT. The Arm® Cortex®-M0 supports both sleep and deep-sleep low-power modes. The deep-sleep mode supports clock gating to limit standby power even further.

Firmware debug support includes 4 breakpoint and 2 watch-point unit comparators using the serial wire debug (SWD) protocol. The serial wire debug mechanism can be disabled to prevent device access to the firmware in the field.

Electrical Characteristics

Table 19 Microcontroller Electrical Characteristics

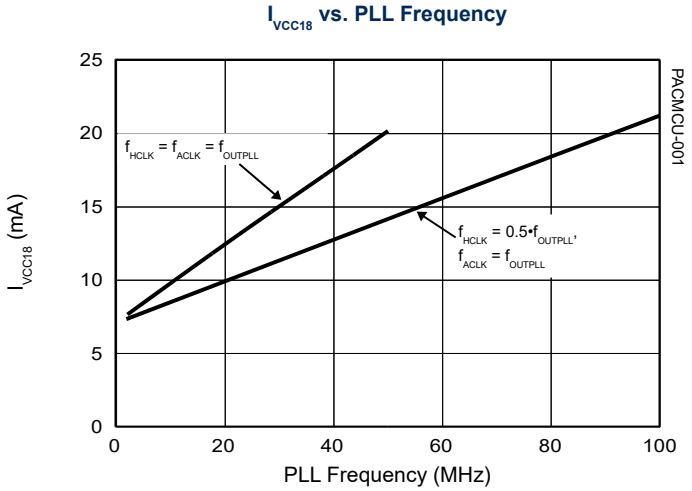
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{HCLK}	Microcontroller clock	HCLK			50	MHz
$I_{OP;VSYS}$	V_{SYS} operating supply current	f_{FRCLK} = f_{HCLK} = f_{ACLK} = ROSC 11b, PLL disabled, CPU halt; other clock sources, ADC, timers, and serial interface disabled	2.5[1]	3.4	7	mA
		f_{FRCLK} = f_{HCLK} = f_{ACLK} = ROSC 01b, PLL disabled, CPU halt; other clock sources, ADC, timers, and serial interface disabled	3.0[1]	5.3	9.5	
		f_{FRCLK} = f_{HCLK} = f_{ACLK} = ROSC 01b, PLL disabled, CPU halt; other clock sources, ADC, timers, and serial interface disabled	4.1[1]	5.3	9.5	
		f_{FRCLK} = f_{HCLK} = f_{ACLK} = ROSC 01b, PLL disabled, CPU halt; other clock sources, ADC, timers, and serial interface disabled	7.4[1]	9	15	
		f_{FRCLK} = f_{HCLK} = f_{ACLK} = CLKREF, PLL disabled, CPU halt; other clock sources, ADC, timers, and serial interface disabled	1.5[1]	2.3	4.4	
		f_{FRCLK} = 4MHz CLKREF, f_{HCLK} = 50MHz, f_{ACLK} = f_{OUTPLL} = 100MHz, CPU halt; other clock sources, ADC, timers, and serial interface disabled	3.6[1]	4.5	6.7	
		f_{FRCLK} = 4MHz CLKREF, f_{HCLK} = 50MHz, f_{ACLK} = f_{OUTPLL} = 100MHz, CPU halt; other clock sources, ADC, timers, and serial interface disabled	20.9[1]	23.3	26.5	
$I_{Q;VCCIO}$	VCCIO quiescent supply current			0.02		mA

(V_{SYS} = V_{CCIO} = 5V, V_{CC33} = 3.3V, V_{CC18} = 1.8V, and T_A = -40°C to 105°C unless otherwise specified.)

[1] All minimum operating supply current values are for room temperature only

Typical Performance Characteristics

Figure 20 Arm® Cortex®-M0 Microcontroller Core



(V_{SYS} = V_{CCIO} = 5V, V_{CC33} = 3.3V, V_{CC18} = 1.8V, and T_A = 25°C unless otherwise specified.)

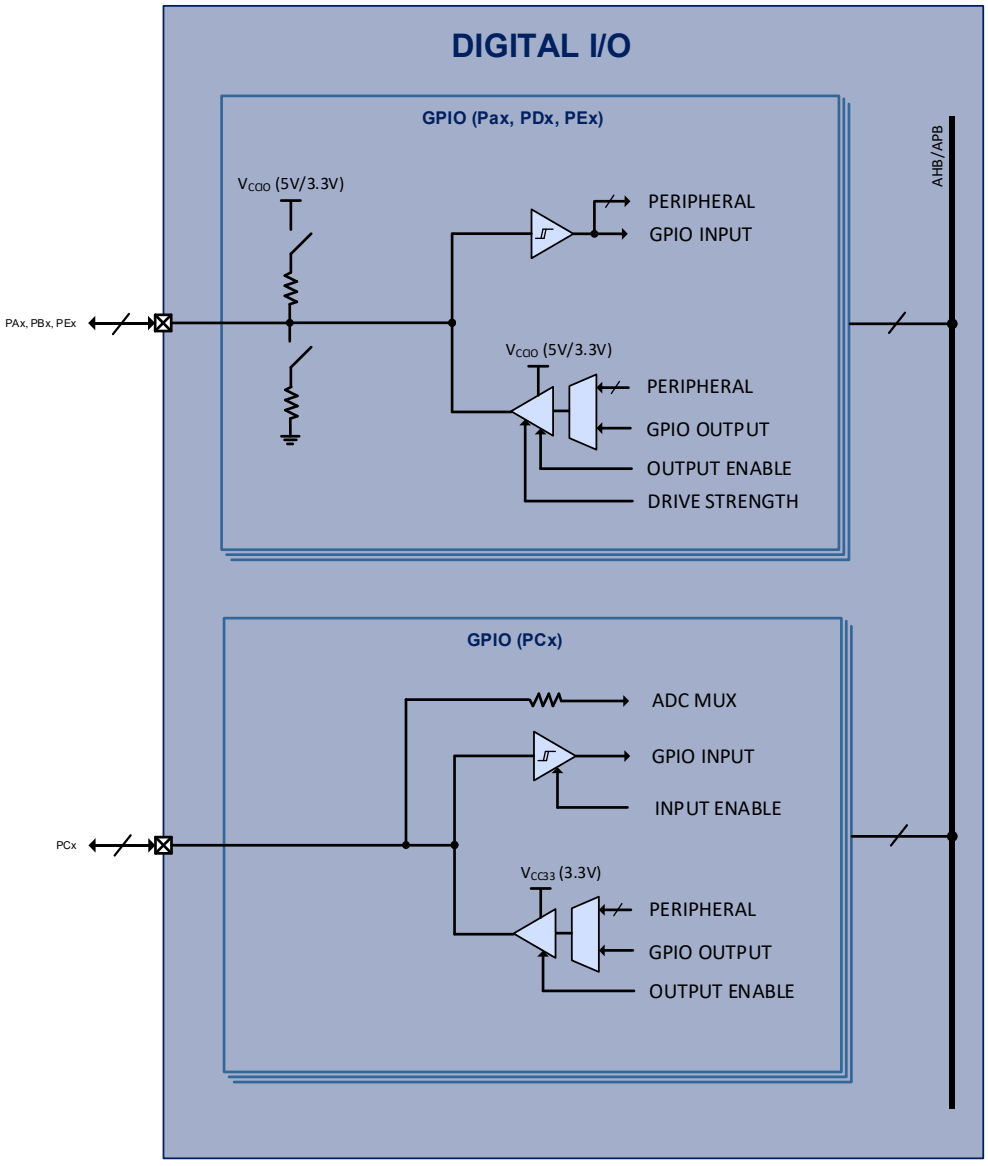
I/O Controller

Features

- 5V-compliant I/O PDx, PEx
- 3.3V-compliant I/O PCx
- Configurable drive strength on PDx, PEx
- Configurable pull-up or pull-down on PDx, PEx

Block Diagram

Figure 21 I/O Controller Block Diagram



Functional Description

The PAC can support up to 4 ports with 8 I/Os each from PAx, PCx, PDx, and PEx, in addition to the I/Os on the analog front end. All PAx, PCx, PDx, and PEx ports have interrupt capability with configurable interrupt edge.

PAx, PDx, and PEx I/Os use V_{CCIO} as the I/O supply voltage that is 5V on default parts (and 3.3V available from factory). The drive current can be configured as 8mA or 16mA. They also support weak pull-up and pull-down to save external components.

PCx uses V_{CC33} as its I/O supply voltage. The drive current is fixed to 8mA. PC0 to PC5 are also associated with analog inputs AD0 to AD5 to the ADC.

GPIO Current Injection

Under normal operation, there should not be current injected into the GPIOs on the device due to the GPIO voltage below ground or above the GPIO supply.[2] Current injected occurs when the GPIO pin voltage is less than -0.3V or when greater than GPIO supply + 0.3V.

In order provide a robust solution when this situation occurs, this device allows a small amount of injected current into the GPIO pins, to avoid excessive leakage or device damage.

For information on the GPIO current injection thresholds, see the absolute maximum parameters for this device.

Sustained operation with the GPIO pin voltage greater than the GPIO supply or when the GPIO pin voltage is less than -0.3V may result in reduced lifetime of the device. GPIO current injection should only be a temporary condition.

[2] VCC33 is the supply for any PC GPIO pin and VCCIO is the supply for any other GPIO pins.

Electrical Characteristics

Table 20 GPIO Electrical Characteristics

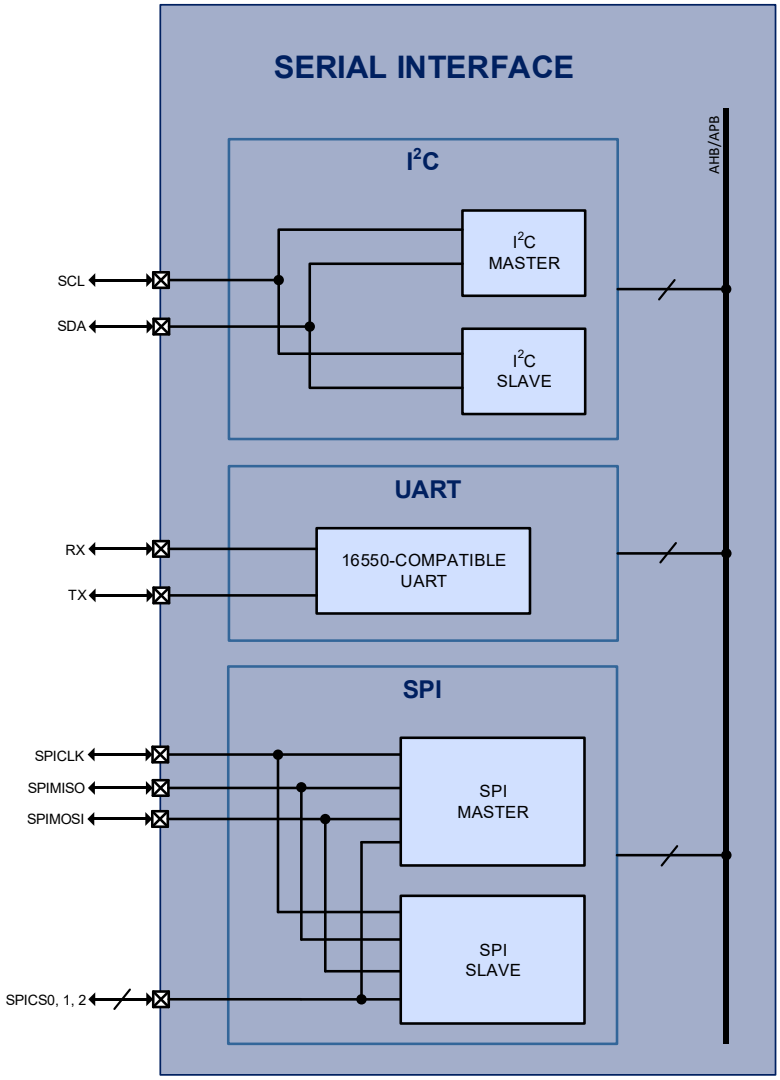
Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
PAx, PDx, PEx (5V Operation)							
V_{IH}	High-level input voltage	V_{CCIO} = 5V		3			V
V_{IL}	Low-level input voltage	V_{CCIO} = 5V				0.8	V
I_{OL}	Low-level output sink current	V_{CCIO} = 5V, V_{OL} = 0.4V	Drive strength setting = 0b	7			mA
			Drive strength setting = 1b	15			
I_{OH}	High-level output source current	V_{CCIO} = 5V, V_{OH} = 2.4V	Drive strength setting = 0b			-7	mA
			Drive strength setting = 1b			-15	
R_{PU}	Weak pull-up resistance	V_{CCIO} = 5V		53	66	87	kΩ
R_{PD}	Weak pull-down resistance	V_{CCIO} = 5V		63	108	244	kΩ
I_{IL}	Input leakage current	T_A = 125°C		-10	0	10	µA
PAx, PDx, PEx (3.3V Operation)							
V_{IH}	High-level input voltage	V_{CCIO} = 3.3V		2			V
V_{IL}	Low-level input voltage	V_{CCIO} = 3.3V				0.8	V
I_{OL}	Low-level output sink current	V_{CCIO} = 3.3V, V_{OL} = 0.4V	Drive strength setting = 0b	4			mA
			Drive strength setting = 1b	8			
I_{OH}	High-level output source current	V_{CCIO} = 3.3V, V_{OH} = 2.4V	Drive strength setting = 0b			-4	mA
			Drive strength setting = 1b			-8	
R_{PU}	Weak pull-up resistance	V_{CCIO} = 3.3V		47	74	104	kΩ
R_{PD}	Weak pull-down resistance	V_{CCIO} = 3.3V		50	84	121	kΩ
I_{IL}	Input leakage current	T_A = 125°C		-10	0	10	µA
PCx (3.3V Operation)							
VIH	High-level input voltage	V_{CC33} = 3.3V		2			V
VIL	Low-level input voltage	V_{CC33} = 3.3V				0.8	V
IOL	Low-level output sink current	V_{CC33} = 3.3V, V_{OL} = 0.4V		7			mA
IOH	High-level output source current	V_{CC33} = 3.3V, V_{OH} = 2.4V				-7	mA
IIL	Input leakage current	T_A = 125°C		-10	0	10	µA

(V_{SYS} = V_{CCIO} = 5V, V_{CC33} = 3.3V, V_{CC18} = 1.8V, and T_A = -40°C to 105°C unless otherwise specified.)

Serial Interface

Block Diagram

Figure 22 Serial Interface Block Diagram



Functional Description

The device has up to three serial interfaces: I²C, UART, and SPI.

I²C Controller

The I²C controller is a configurable peripheral that can support various modes of operation:

- I²C master operation
  - Normal mode (100kHz), fast mode (400kHz), or fast mode plus (1MHz)
  - Single and multi-master
  - Synchronization (multi-master)
  - Arbitration (multi-master)
  - 7-bit or 10-bit slave addressing
- I²C slave operation
  - Normal mode (100kHz), fast mode (400kHz), or fast mode plus (1MHz)
  - Clock stretching
  - 7-bit or 10-bit slave addressing

The I²C peripheral may operate either by polling or can be configured to be interrupt driven for both receive and transmit data.

UART Controller

The UART peripheral is a configurable peripheral that can support various features and modes of operation:

- Programmable clock selection
- National Instruments PC16550D compatible
- 16-deep transmit and receive FIFO and fractional clock divisor
- Up to 3.125Mbps communication speed (with HCLK = 50MHz)

The UART peripheral may operate either by polling or can be configured to be interrupt driven for both receive and transmit data.

SPI Controller

The device contains an SPI controller that can each be used in either master or slave operation, with the following features:

- SPI master operation
  - Control of up to three different SPI slaves
  - Operation up to 25MHz
  - Flexible multiple transmit mode for variable-size SPI data with user-defined chip-select behavior

- Chip select “shaping” through programmable additional delay for chip-select setup, hold and wait time for back-to-back transfers

- SPI master or slave operation
  - Supports clock phase and polarity control
  - Data transmission/reception can be on 8-, 16-, 24- or 32-bit boundary
  - Selectable data bit ordering (LSB or MSB first)
  - Programmable chip select polarity
  - Selectable “auto-retransmit” mode

The SPI peripheral may operate either by polling or can be configured to be interrupt driven for both receive and transmit data.

Dynamic Characteristics

Table 21 Serial Interface Dynamic Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I2C						
f_{I2CCLK}	I2C input clock frequency	Standard mode (100kHz)	2.8			MHz
		Fast mode (400kHz)	2.8			MHz
		Fast mode plus (1MHz)	6.14			MHz
UART						
$f_{UARTCLK}$	UART input clock frequency				f_{HCLK}/16	MHz
	UART baud rate	f_{HCLK} = 50MHz			3.125	Mbps
SPI						
f_{SPICLK}	SPI input clock frequency	Master mode			f_{HCLK}/2	MHz
		Slave mode			f_{HCLK}/2	MHz

(V_{SYS} = V_{CCIO} = 5V, V_{CC33} = 3.3V, V_{CC18} = 1.8V, and T_A = -40°C to 105°C unless otherwise specified.)

Table 22 I2C Dynamic Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{SCL}	SCL clock frequency	Standard mode	0		100	kHz
		Fast mode	0		400	
		Fast mode plus	0		1000	
t_{LOW}	SCL clock low	Standard mode	4.7			µs
		Fast mode	1.3			
		Fast mode plus	0.5			
t_{HIGH}	SCL clock high	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus	0.26			
$t_{HD;STA}$	Hold time for a repeated START condition	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus	0.26			
$t_{SU;STA}$	Set-up time for a repeated START condition	Standard mode	4.7			µs
		Fast mode	0.6			
		Fast mode plus	0.26			
$t_{HD;DAT}$	Data hold time	Standard mode	0		3.45	µs
		Fast mode	0		0.9	
		Fast mode plus	0			
$t_{SU;DAT}$	Data set-up time	Standard mode	250			ns
		Fast mode	100			
		Fast mode plus	50			
$t_{SU;STO}$	Set-up time for STOP condition	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus	0.26			
t_{BUF}	Bus free time between a STOP and START condition	Standard mode	4.7			µs
		Fast mode	1.3			
		Fast mode plus	0.5			
t_r	Rise time for SDA and SCL	Standard mode			1000	ns
		Fast mode	20		300	
		Fast mode plus			120	
t_f	Fall time for SDA and SCL	Standard mode			300	ns
		Fast mode			300	
		Fast mode plus			120	
C_b	Capacitive load for each bus line	Standard mode, fast mode			400	pF
		Fast mode plus			550	

Figure 23 I2C Timing Diagram

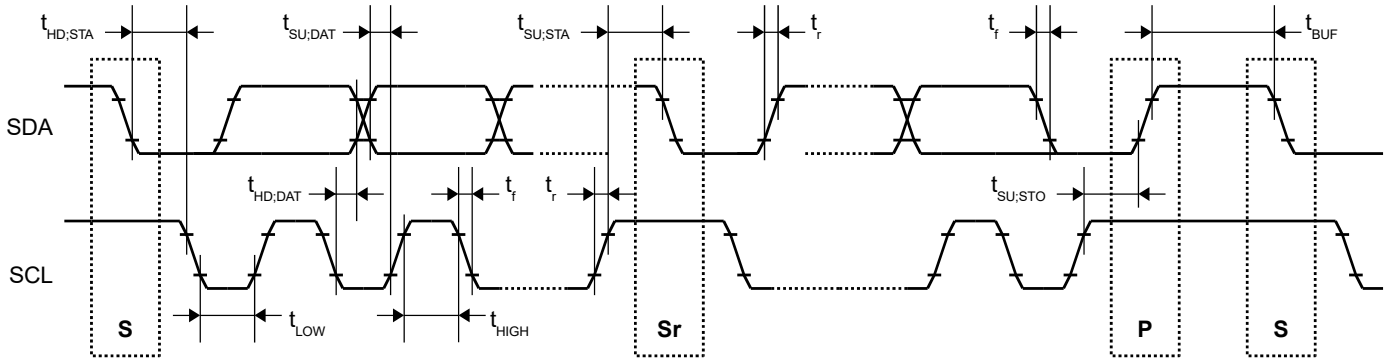
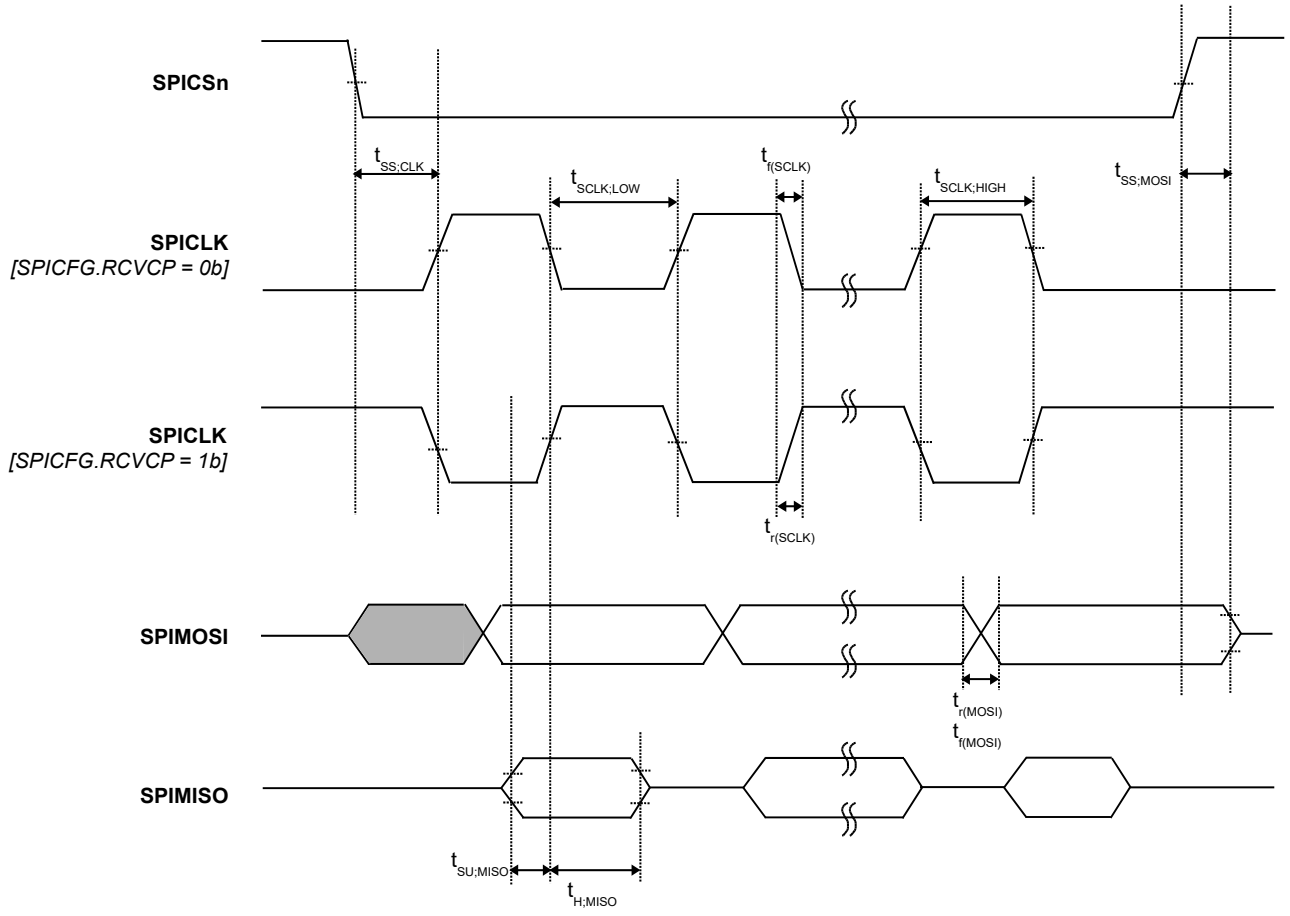


Table 23 SPI Dynamic Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{SCLK;HIGH}$	SPICLK Input High Time	SPICLK = 25MHz	30			ns
$t_{SCLK;LOW}$	SPICLK Input Low Time		30			ns
$t_{SS;SCLK}$	SPICSn to SPICLK Time		120			ns
$t_{SS;MOSI}$	SPICSn to SPIMISO High-impedance time		10		50	ns
$t_{r(SCLK)}$	SPICLK Rise Time			10	25	ns
$t_{f(SCLK)}$	SPICLK Fall Time			10	25	ns
$t_{r(MOSI)}$	SPIMISO Rise Time			10	25	ns
$t_{f(SMOSI)}$	SPIMISO Fall Time			10	25	ns
$t_{SU;MISO}$	SPIMISO Setup Time		20			ns
$t_{H;MISO}$	SPIMISO Hold Time		20			ns

Figure 24 SPI Timing Diagram



Timers

Block Diagrams

Figure 25 PWM Timers Block Diagram

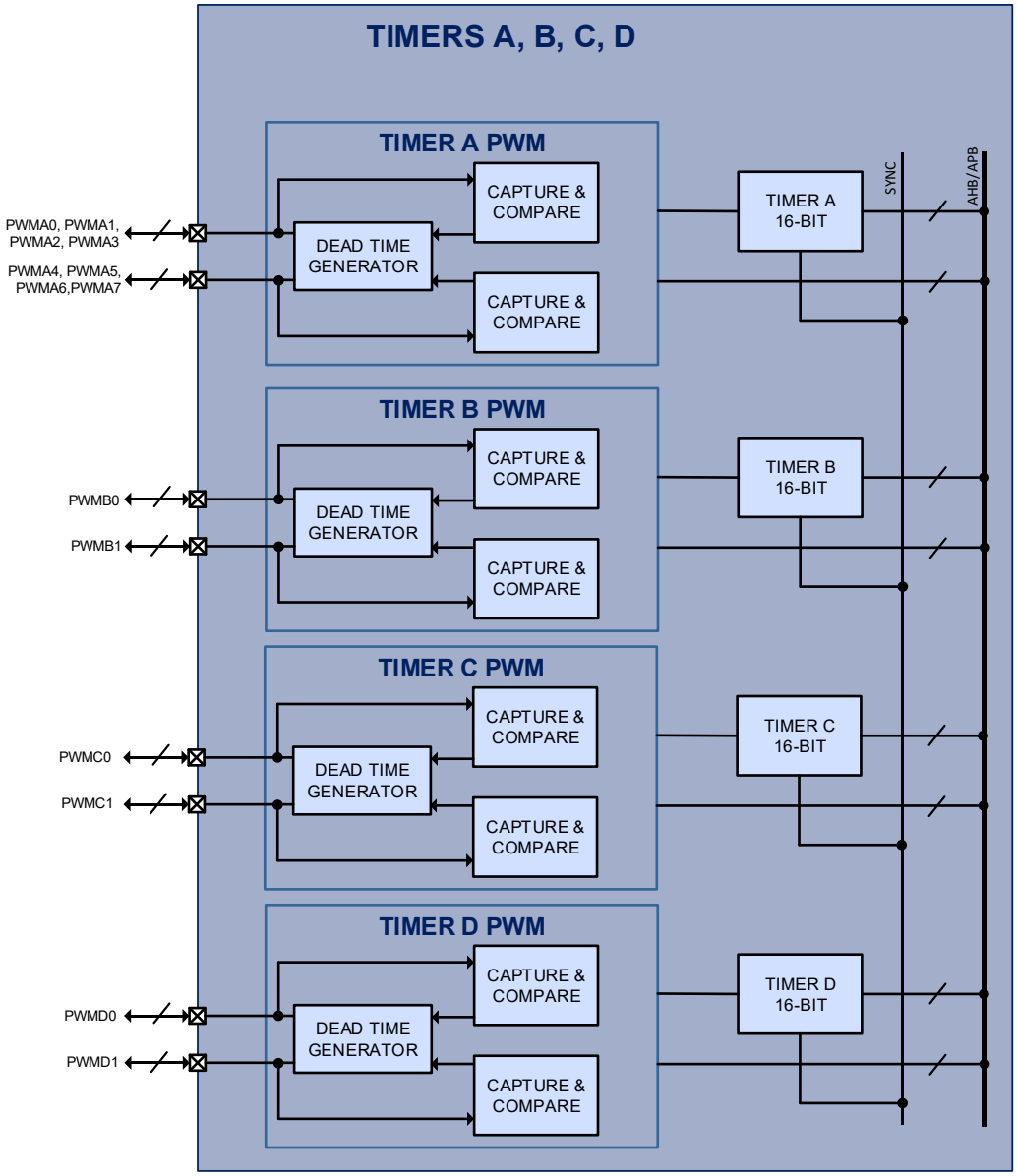


Figure 26 AFE Watchdog and Wake-up Timer Block Diagram

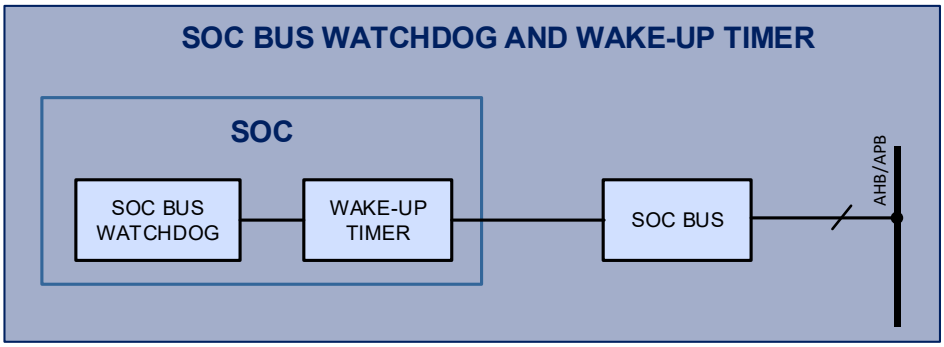
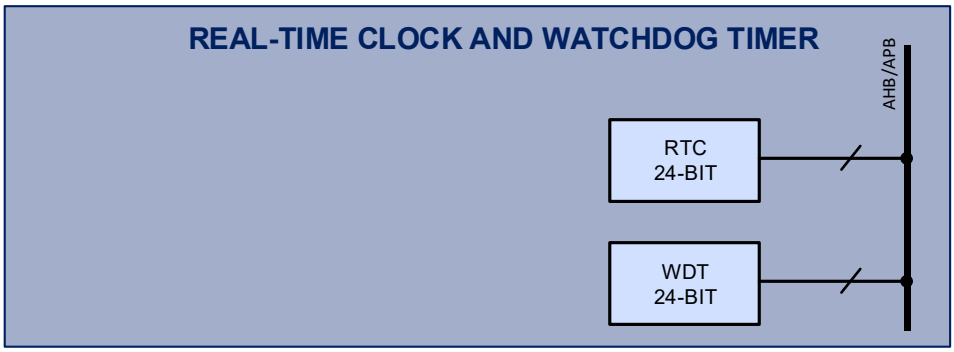


Figure 27 Real-time Clock and Watchdog Timer Block Diagram



Functional Description

The device includes 9 timers: timer A, timer B, timer C, timer D, watchdog timer 1 (WDT), watchdog timer 2, wake-up timer, real-time clock (RTC), and SysTick timer. The device supports up to 14 different PWM signals and has up to 7 dead-time controllers. Timers A, B, C and D can be concatenated to synchronize to a single clock and start/stop signal for applications that require a synchronized timer period between timers.

Timer A

Timer A is a general purpose 16-bit timer with 8 PWM/capture and compare units. It has 4 pairs of PWM signals going into 4 dead-time controllers. Timer A can be concatenated with timers B, C, and D to synchronize the PWM/capture and compare units. It can use either ACLK or HCLK as clock input with an additional clock divider from /1 to /128.

Timer B

Timer B is a general purpose 16-bit timer with 2 PWM/capture and compare units. It has one pair of PWM signals going into one dead-time controller, as well as 2 additional compare units that can be used for additional system time bases for interrupts. Timer B can be concatenated with timers A, C, and D to synchronize the PWM/capture and compare units. It can use either ACLK or HCLK as clock input with an additional clock divider from /1 to /128.

Timer C

Timer C is a general purpose 16-bit timer with 2 PWM/capture and compare units. It has one pair of PWM signals going into one dead-time controller. Timer C can be concatenated with timers A, B, and D to synchronize the PWM/capture and compare units. It can use either ACLK or HCLK as clock input with an additional clock divider from /1 to /128.

Timer D

Timer D is a general purpose 16-bit timer with 2 PWM/capture and compare units. It has one pair of PWM signals going into one dead-time controller. Timer D can be concatenated with timers A, B, and C to synchronize the PWM/capture and compare units. It can use either ACLK or HCLK as clock input with an additional clock divider from /1 to /128.

Watchdog Timer

The 24-bit watchdog timer (WDT) can be used for long time period measurements or periodic wake up from sleep mode. The watchdog timer can be used as a system watchdog to reset the MCU, or as an interval timer, or both. The watchdog timer can use either FRCLK or FCLK as clock input with an additional clock divider from /2 to /65536.

CAFE Watchdog Timer

There is a second watchdog timer in the AFE that can be used to reset both the MCU and AFE. If this timer expires, it will trigger a full device reset.

Wake-Up Timer

The wake-up timer can be used for very low power hibernate and sleep modes to wake up the micro controller periodically. It can be configured to be 125ms, 250ms, 500ms, 1s, 2s, 4s, or 8s.

Real-Time Clock

The 24-bit real-time clock (RTC) can be used for time measurements when an accurate clock source is used. This timer can also be used as an internal timer or for periodic wake up from sleep mode. The RTC uses FRCLK as clock input with an additional clock divider from /2 to /65536.

Application Block Diagrams

Figure 28 PAC22140 Application Block Diagram

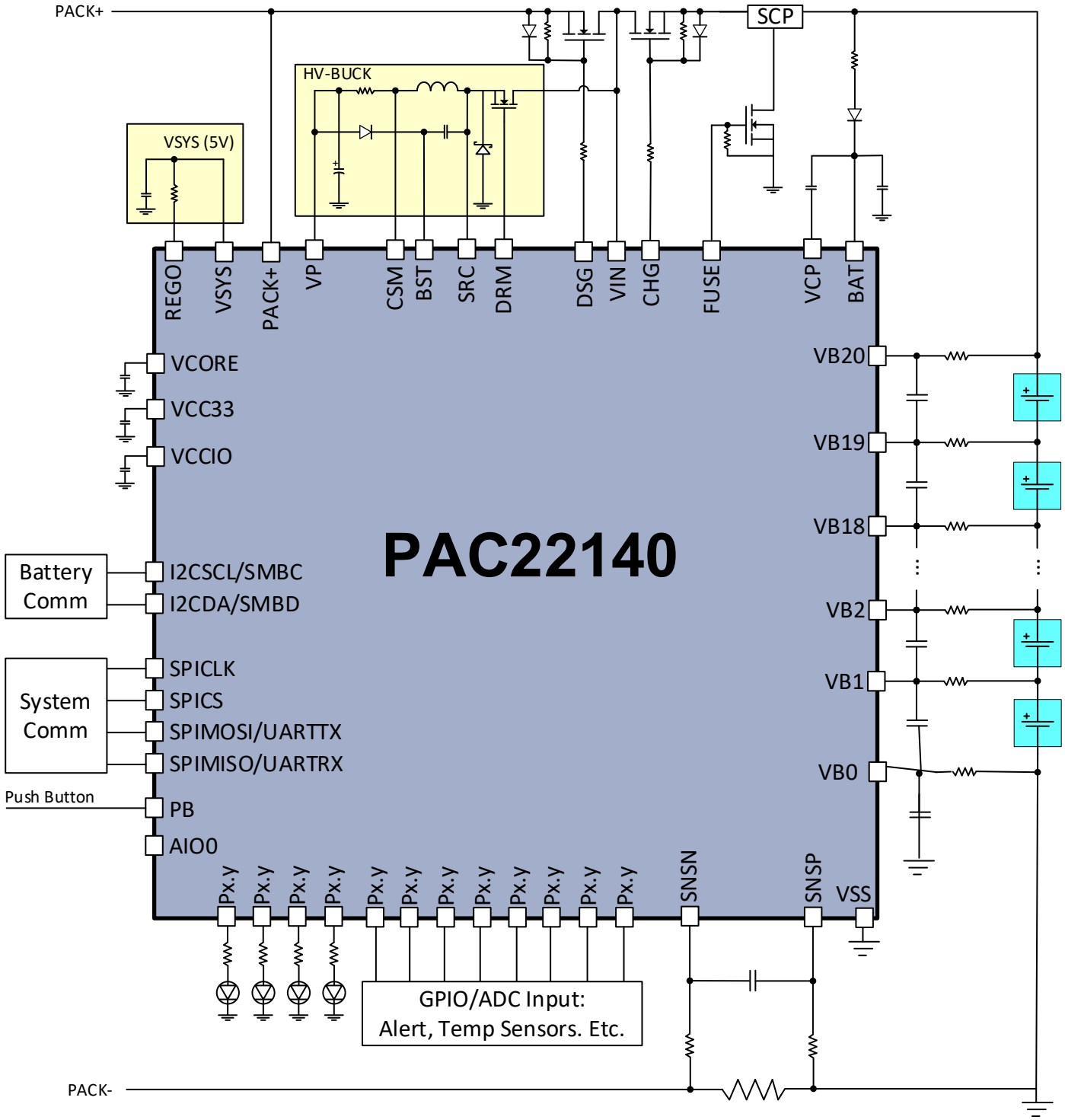
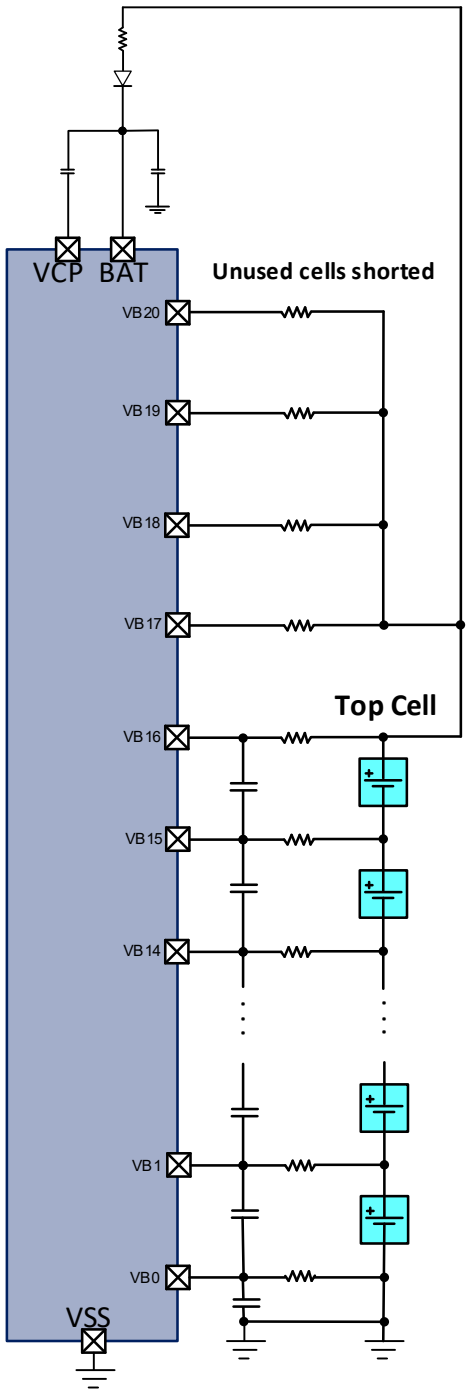


Figure 29 PAC22140 Cell Count Reduction Application Diagram for 16s



The PAC22140 can monitor a 10-series to 20 series battery pack. In the actual application, the number of used cells may be less than 20 cells, in the figure above is a 16s example. When using less than 20 cells, the unused cells and corresponding VBx pins should be shorted together. The Top of the highest cell should be tied to the VBAT connection as shown.

Thermal Characteristics

Table 24 Thermal Characteristics

SYMBOL	PARAMETER	VALUE	UNIT
T_A	Operating ambient temperature range	-40 to 105	°C
T_J	Operating junction temperature range	-40 to 125	°C
T_{STG}	Storage temperature range	-55 to 150	°C
	Lead temperature (Soldering, 10 seconds)	300	°C
Θ_{JC}	Junction-to-case thermal resistance	2.897	°C/W
Θ_{JA}	Junction-to-ambient thermal resistance	23.36	°C/W

Pin Configuration and Description

Figure 30 Pin Diagram – Top View

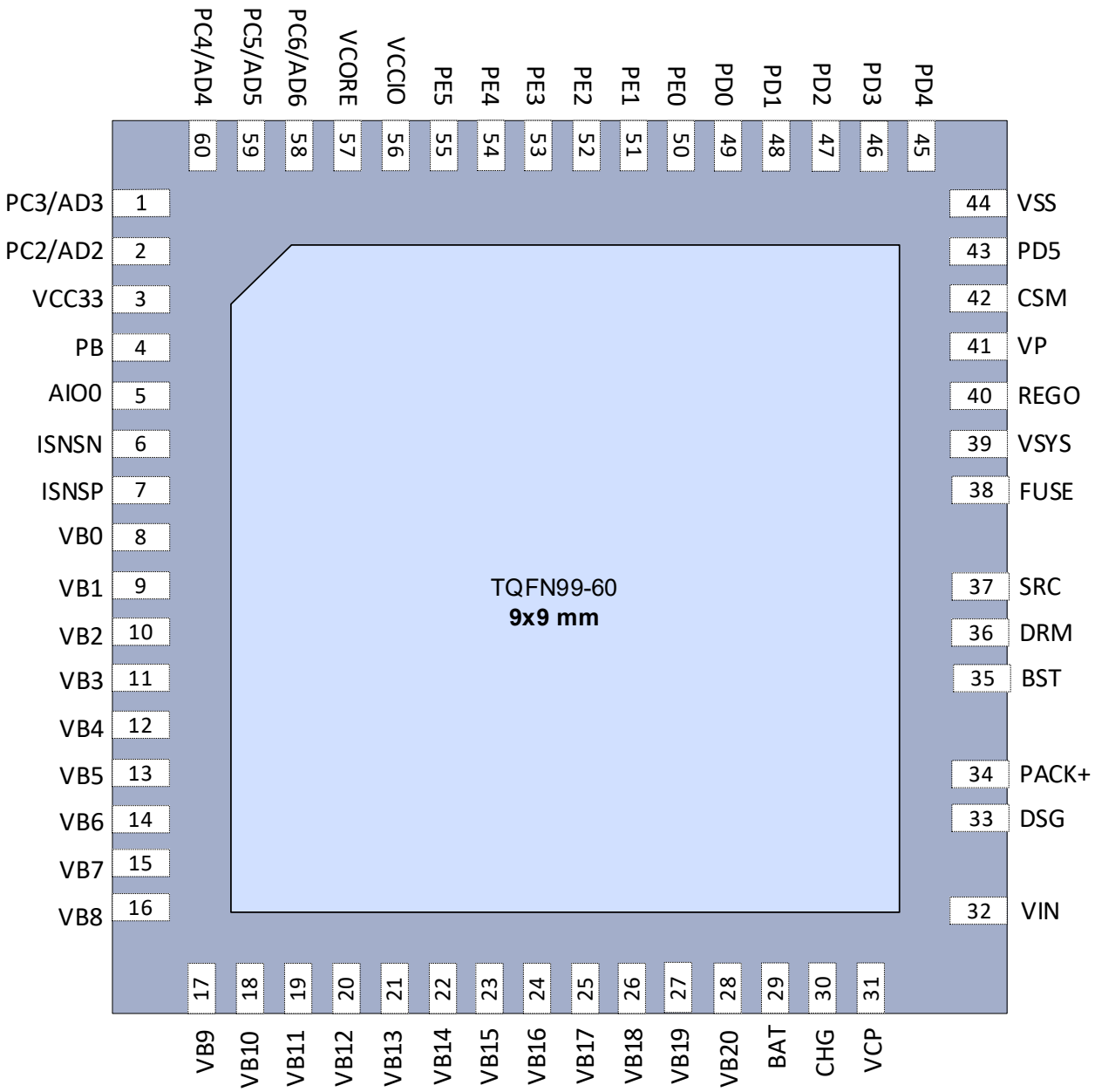


Table 25 – Pin Descriptions

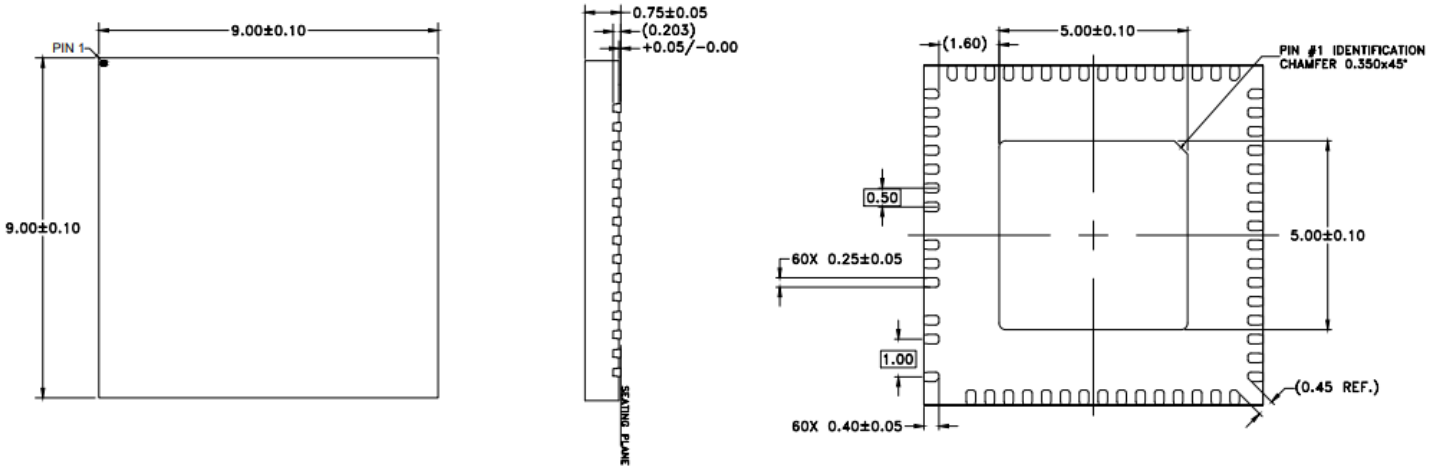
Pin Number	Label	Description
1	PC3/AD3	IO port PC3 or ADC channel AD3.
2	PC2/AD2	IO port PC2 or ADC channel AD2.
3	VCC33	Internally generated 3.3V power supply. Connect to a 10V/2.2µF or higher ceramic capacitor from VCC33 to VSS close to the device.
4	PB	Push Button Sense Input
5	AIO0	Analog I/O 0
6	ISNSN	Current sense, negative terminal.
7	ISNSP	Current sense, positive terminal.
8	VB0	Sense voltage input for the bottom of the battery stack.
9	VB1	Sense voltage input for the 1st cell in the battery stack.
10	VB2	Sense voltage input for the 2nd cell in the battery stack.
11	VB3	Sense voltage input for the 3rd cell in the battery stack.
12	VB4	Sense voltage input for the 4th cell in the battery stack.
13	VB5	Sense voltage input for the 5th cell in the battery stack.
14	VB6	Sense voltage input for the 6th cell in the battery stack.
15	VB7	Sense voltage input for the 7th cell in the battery stack.
16	VB8	Sense voltage input for the 8th cell in the battery stack.
17	VB9	Sense voltage input for the 9th cell in the battery stack.
18	VB10	Sense voltage input for the 10th cell in the battery stack.
19	VB11	Sense voltage input for the 11th cell in the battery stack.
20	VB12	Sense voltage input for the 12th cell in the battery stack.
21	VB13	Sense voltage input for the 13th cell in the battery stack.
22	VB14	Sense voltage input for the 14th cell in the battery stack.
23	VB15	Sense voltage input for the 15th cell in the battery stack.
24	VB16	Sense voltage input for the 16th cell in the battery stack.
25	VB17	Sense voltage input for the 17th cell in the battery stack.
26	VB18	Sense voltage input for the 18th cell in the battery stack.
27	VB19	Sense voltage input for the 19th cell in the battery stack.
28	VB20	Sense voltage input for the 20th cell in the battery stack.
29	BAT	Battery Stack Voltage. Connect to the top of the battery stack.
30	CHG	Charge FET gate drive output.
31	VCP	High-Voltage Charge Pump output. Connect a 0.47µF VP rated capacitor between VCP and VIN close to the device.
32	VIN	High-Voltage Buck Regulator supply controller input. Connect a 1µF 200V or higher value ceramic capacitor, and a 0.1µF 200V ceramic capacitor and in parallel with a 22µF 200V or higher electrolytic capacitor from VIN to VSS. This pin requires good capacitive bypass to VSS, so the ceramic capacitor must have a trace less than 10mm from the pin.
33	DSG	Discharge FET gate drive output.
34	PACK+	Battery Pack Positive Output. Connect to the positive terminal of the battery charger supply or load.
35	BST	High-Voltage Buck Regulator bootstrap input. Connect a 2.2µF or higher value ceramic capacitor from BST to SRC with a shorter than 10mm trace from the pin.

Pin Number	Label	Description
36	DRM	High-Voltage Buck Regulator Switching supply driver output. Connect to the base or gate of the external N-channel MOSFET.
37	SRC	High-Voltage Buck Regulator Source. Connect to the source of the high-side power MOSFET of the high-voltage buck regulator.
38	FUSE	FUSE Low-Side FET gate drive output.
39	VSYS	Internally generated 5V power supply. Connect to a 10V/4.7µF ceramic capacitor from VSYS to VSS close to the device.
40	REGO	VSYS regulator output.
41	VP	Main power supply. Provides power to the power drivers as well as voltage feedback path for the switching supply. Connect a properly sized supply bypass capacitor in parallel with a 10µF ceramic capacitor in parallel with a 100µF aluminum capacitor from VP to VSS for voltage loop stabilization. If the switching frequency of the HV-BUCK is >= 200kHz, then the 100µF aluminum capacitor can be replaced with 47µF, but the efficiency will be worse. This pin requires good capacitive bypass to VSS, so the ceramic capacitor must have a trace less than 10mm from the pin.
42	CSM	High-Voltage Buck Regulator Switching supply current sense input. Connect to the positive side of the current sense resistor.
43	PD5	IO port PD5 or Timer A, PWM/Capture Unit 5 or Timer C, PWM/Capture Unit 1.
44	VSS	Ground.
45	PD4	IO port PD4 or Timer D, PWM/Capture Unit 1
46	PD3	IO port PD3 or Timer A, PWM/Capture Unit 5 or Timer C, PWM/Capture Unit 1.
47	PD2	IO port PD2 or SWD Serial Data.
48	PD1	IO port PD1 or SWD Serial Clock or External Clock Input
49	PD0	IO port PD0 or SWD Serial Data.
50	PE0	IO port PE0 or SPICLK I/O.
51	PE1	IO port PE1 or SPI Master-out, slave-in (MOSI) or UART Transmit Output.
52	PE2	IO port PE2 or SPI Master-in, slave-out (MISO) or UART Receive Input.
53	PE3	IO port PE3 or SPI chip-select 0 or Reset input 1 (active-low).
54	PE4	IO port PE4 or SPI chip-select 1 or I2C Serial Clock.
55	PE5	IO port PE5 or SPI chip-select 2 or I2C Serial Data.
56	VCCIO	Internally generated digital I/O 3.3V power supply. Connect a 2.2µF or higher value ceramic capacitor from VCCIO to VSS.
57	VCORE	Internally generated 1.9V core power supply. Connect a 2.2µF or higher value ceramic capacitor from VCORE to VSS.
58	PC6/AD6	IO port PC6 or ADC channel AD6.
59	PC5/AD5	IO port PC5 or ADC channel AD5.
60	PC4/AD4	IO port PC4 or ADC channel AD4.

Mechanical Information

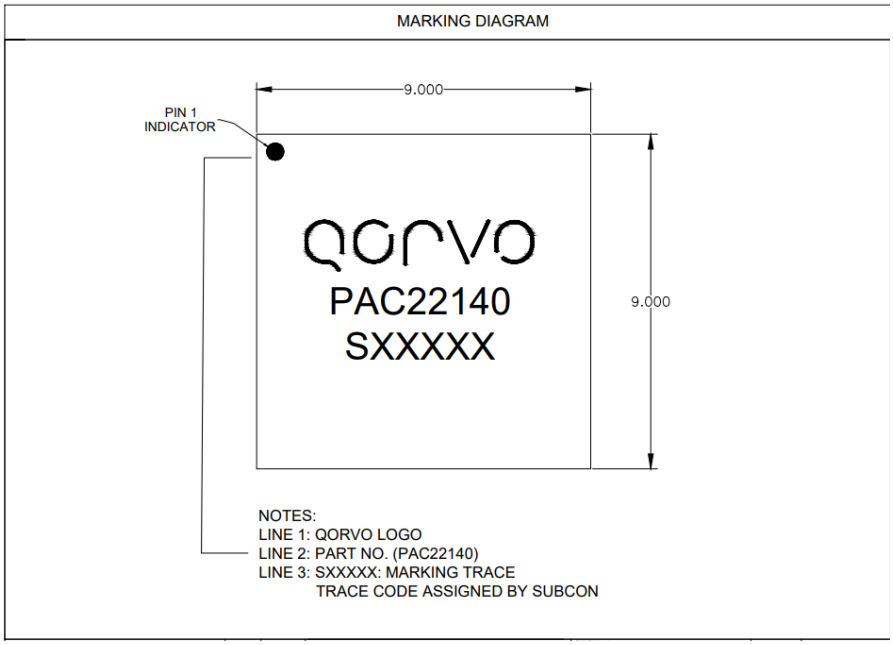
Package Marking and Dimensions

Marking: Part number – PAC22140



Notes:
1. All dimensions are in mm. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

Package Marking



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1A	ESDA/JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!

ESD sensitive device

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Revision History

Revision	Description
1.1	**Initial Web Release**
1.2	**Updated to align with PAC25140. IADC spec change**
1.3	**Updated Cell Error, Add VIN current power modes, VIN pin description cap change**
1.4	**Updated CAFÉ figure**

Product Compliance

This part complies with RoHS directive 2011/65/EU as amended by (EU) 2015/863.

This part also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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